**NXP Semiconductors**
Data Sheet: Advance Information

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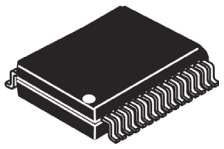
# Dual 24 V, 22 mOhm high-side switch

**22XS4200**

**HIGH-SIDE SWITCH**

The 22XS4200 device is part of a 24 V dual high-side switch product family with integrated control, and a high number of protective and diagnostic functions. It is designed for truck and bus applications. The low $R_{DS(on)}$ channels (<22 mΩ) can control different load types; bulbs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit serial peripheral interface (SPI), allowing easy integration into existing applications. This device is powered by SMARTMOS technology.

Both channels can be controlled individually by external/internal clock signals, or by direct inputs. Using the internal clock allows fully autonomous device operation. Programmable output voltage slew rates (individually programmable) helps improve electromagnetic compatibility (EMC) performance. To avoid shutting off the device upon inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Switching current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a Fail-safe operation mode, but remains operational, controllable, and protected.



**BEK SUFFIX (PB-FREE)**
**98ASA00368D**
**32 PIN SOIC (10 mm X 11 mm)**

**CEK SUFFIX (PB-FREE)**
**98ASA00894D**
**32 PIN SOIC (10 mm X 11 mm)**

### Features

- Two fully-protected 22 mΩ (at 25 °C) high-side switches
- Up to 4.2 A steady state current per channel
- Separate bulb and DC motor latched overcurrent handling
- Individually programmable internal/external PWM clock signals
- Overcurrent, short-circuit, and overtemperature protection with programmable autoretry functions
- Accurate temperature and current sensing
- Open load detection (channel in OFF and ON state), also for LED applications (7.0 mA typ.)
- Normal operating range: 8.0 V to 36 V, extended range: 6.0 V to 58 V
- 3.3 V and 5.0 V compatible 16-bit SPI port for device control, configuration and diagnostics at rates up to 8.0 MHz

### Applications

- Truck, bus and 24 V transportation systems
- Resistive, capacitive, and inductive loads

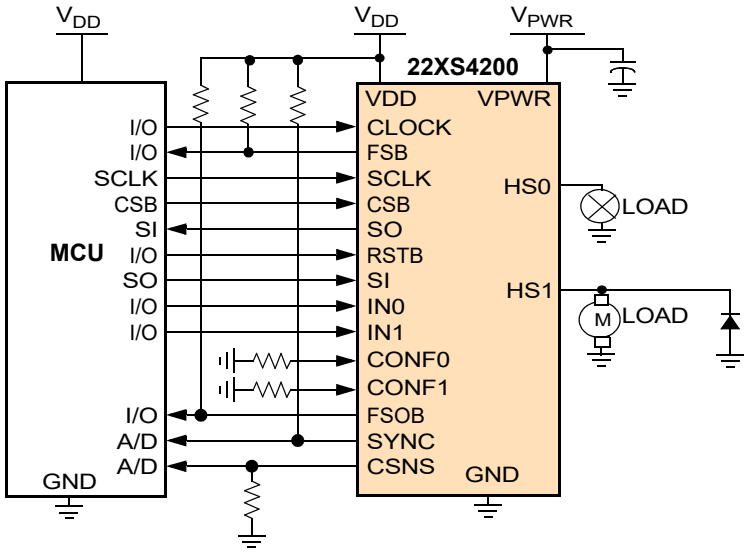



**Figure 1. Simplified application diagram**

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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# Table of Contents


1 Orderable parts . . . 3
2 Internal block diagram . . . 4
3 Pin assignment . . . 5
4 Electrical characteristics . . . 7
4.1 Maximum ratings . . . 7
4.2 Static electrical characteristics . . . 9
4.3 Dynamic electrical characteristics . . . 15
4.4 Timing diagrams . . . 20
5 Functional description . . . 23
5.1 Introduction . . . 23
5.2 Pin assignment and functions . . . 23
5.3 Functional internal block description . . . 26
6 Functional device operation . . . 27
6.1 Operation and operating modes . . . 27
6.3 Logic commands and SPI registers . . . 46
7 Typical applications . . . 54
8 Packaging . . . 56
8.1 Package mechanical dimensions . . . 56
9 Revision history . . . 63

# 1 Orderable parts

**Table 1. Orderable part variations**

| Part number [1] | Temperature ($T_A$) | Package |
|---|---|---|
| MC22XS4200BEK | -40 °C to 125 °C | 32 SOIC-EP |
| MC22XS4200CEK | | |

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

# 2 Internal block diagram

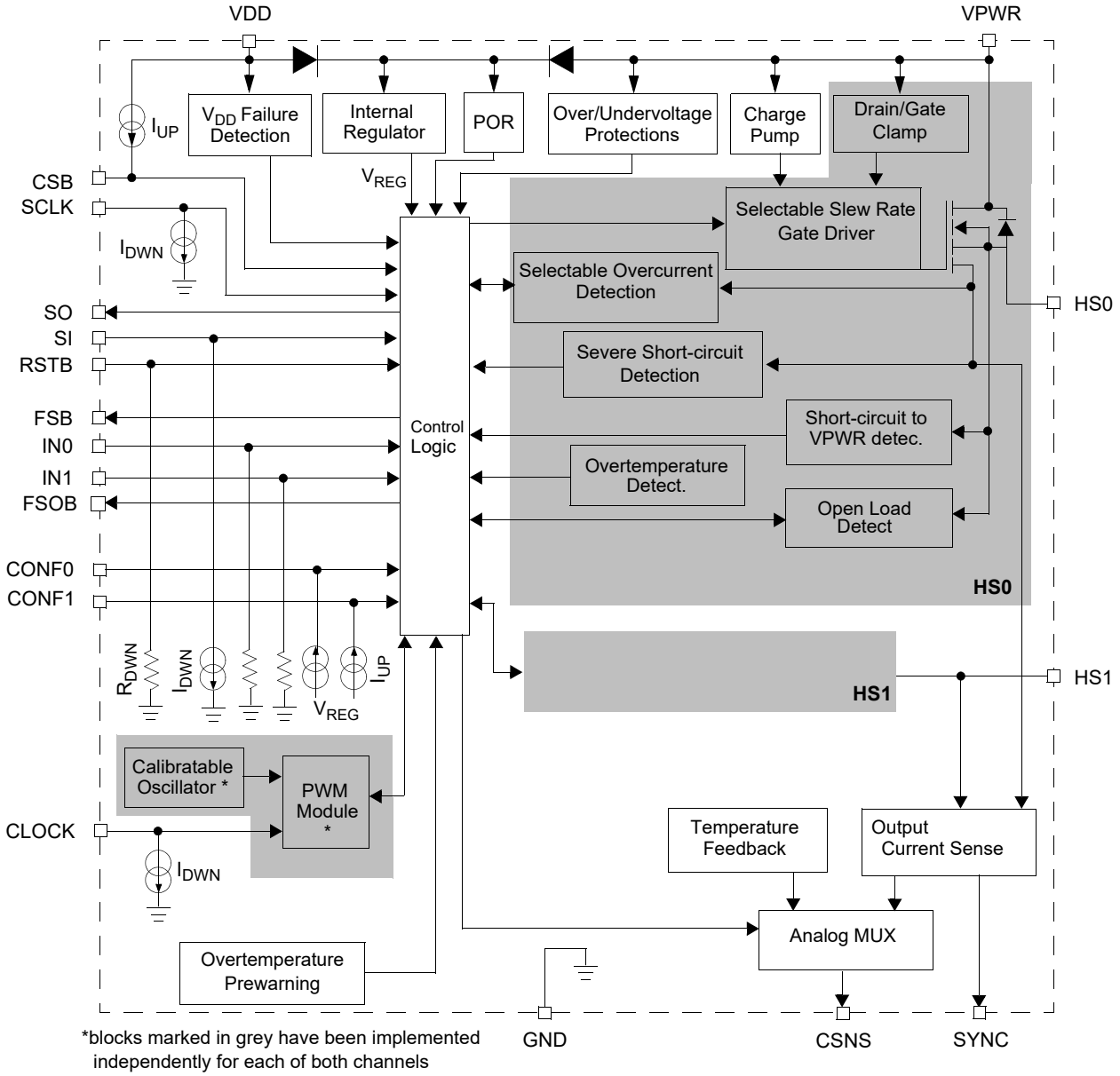



**Figure 2. Internal block diagram**

# 3 Pin assignment

**Transparent Top View**

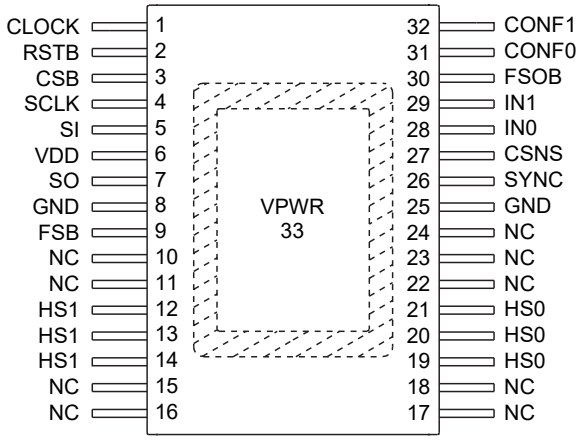



**Figure 3. Device pin assignments**

The function of each pin is described in the section Functional description

**Table 2. 22XS4200 pin description**

| Pin number | Pin name | Function | Formal name | Definition |
|---|---|---|---|---|
| 1 | CLOCK | Input | PWM Clock | The clock input gives the time-base when the device is operated in external clock/internal PWM mode. This pin has an internal pull-down current source. |
| 2 | RSTB | Input | Reset | This input pin is used to initialize the device's configuration - and fault registers. Reset puts the device in Sleep mode (low current consumption) provided it is not stimulated by direct input signals. This pin is connected to GND by an internal pull-down resistor. |
| 3 | CSB | Input | Chip Select (Active Low) | This input pin is connected to the SPI chip-select output of an external microcontroller. CSB is internally pulled up to $V_{DD}$ by a current source $I_{UP}$. |
| 4 | SCLK | Input | Serial Clock | This input pin is to be connected to an external SPI Clock signal. The SCLK pin is internally connected to a pull-down current source $I_{DWN}$. |
| 5 | SI | Input | Serial Input | This input pin receives the SPI input data from an external device (microcontroller or another extreme switch device in case of daisy-chaining). The SI pin is internally connected to a pull-down current source $I_{DWN}$. |
| 6 | VDD | Power | Digital Drain Voltage | This is the positive supply pin of the SPI interface. |
| 7 | SO | Output | Serial Output | This output pin transmits SPI data to an external device (external microcontroller or the SI pin of the next SPI device in case of daisy-chaining). The pin doesn't require external pull-up or pull-down resistors, but a series resistor is recommended to limit current consumption in case of GND disconnection. |
| 8, 25 | GND | Ground | Ground | These pins are the ground for the logic and analog circuitries of the device. For ESD and electrical parameter accuracy purpose, the ground pins must be shorted in the board. |
| 9 | FSB | Output | Fault Status (Active Low) | This open drain output pin (external pull-up resistor to $V_{DD}$ required) is set when the device enters Fault mode (see Fault mode). |
| 10, 11, 15, 16, 17, 18, 22, 23, 24 | NC | N/A | Not connected | These pins may not be connected. |
| 12, 13, 14, 19, 20, 21 | HS1 HS0 | Output | Power Switch Outputs | Output pins of the switches, to be connected to the load. |

**Table 2. 22XS4200 pin description (continued)**

| Pin number | Pin name | Function | Formal name | Definition |
|---|---|---|---|---|
| 26 | SYNC | Output | Output Current Monitoring Synchronization | This output pin is asserted (active low) when the Current Sense (CS) output signal is within the specified accuracy range. Reading the SYNC pin allows the external microprocessor to synchronize to the device when operating in autonomous operating mode. SYNC is open drain and requires a pull-up resistor to $V_{DD}$. |
| 27 | CSNS | Output | Output Current/ Temperature Monitoring | This pin either outputs a current proportional to the channel's output current or a voltage proportional to the temperature of the GND pin (pin 14). Selection between current and temperature sensing, as well as setting the current sensing sensitivity are performed through the SPI interface. An external pull-down resistor must be connected between CSNS and GND. |
| 28, 29 | IN0<br>IN1 | Input | Direct Inputs | The IN[0: 1] input pins are used to directly control the switching state of both switches and consequently the voltage on the HS0: HS1 output pins. The pins are connected to GND by internal pull-down resistors. |
| 30 | FSOB | Output | Fail-safe Output (Active Low) | FSOB is asserted (active-low) upon entering Fail-safe mode (see Functional description) This open drain output requires an external pull-up resistor to $V_{PWR}$. |
| 31, 32 | CONF0<br>CONF1 | Input | Configuration Input | The CONF[0: 1] input pins are used to select the appropriate overcurrent detection profile (bulb/DC motor) for each of both channels. CONF requires a pull-down resistor to GND. |
| 33 | VPWR | Power | Positive Power Supply | This exposed pad connects to the positive power supply and is the drain of both internal MOSFET switches. |

# 4 Electrical characteristics

## 4.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

| Symbol | Parameter | Maximum ratings | Unit | Notes |
|---|---|---|---|---|
| **Electrical ratings** | | | | |
| $V_{PWR}$ | VPWR supply voltage range<br>• Load dump at 25 °C (350 ms)<br>• Reverse battery at 25 °C<br>• Fast negative transient pulses (ISO 7637-2 pulse #1, $V_{PWR}$=28 V & Ri=10 Ω) | <br>58<br>-32<br>-60 | V | |
| $V_{DD}$ | VDD supply voltage range | -0.3 to 5.5 | V | |
| $V_{MAX,LOGIC}$ | Voltage on input pins (except IN[0:1]) and Output pins) (except HS[0:1]) | -0.3 to 5.5 | V | (2) (3) |
| $V_{FSO}$ | Voltage on fail-safe output (FSOB) | -0.3 to 58 | V | |
| $V_{SO}$ | Voltage on SO pin | -0.3 to $V_{DD}$+0.3 | V | |
| $V_{IN,MAX}$ | Voltage (continuous, max. allowable) on IN[0:1] inputs | 58 | V | |
| $V_{HS[0:1]}$ | Voltage (continuous, max. allowable) on output pins (HS [0:1]), | -32 to 58 | V | |
| $I_{HS[0:1]}$ | Rated continuous output current per channel | 4.2 | A | (4) |
| $E_{CL[0:1]_SING}$ | Maximum allowable energy dissipation per channel and two parallel channels, single-pulse method | 36 | mJ | (5) |
| $V_{ESD1}$<br>$V_{ESD2}$<br><br>$V_{ESD3}$<br>$V_{ESD4}$ | ESD voltage<br>• Human body model (HBM) for HS[0:1], VPWR and GND<br>• Human body model (HBM) for other pins<br>• Charge device model (CDM)<br>Package corner pins (1, 13, 19, 20)<br>All other pins | <br>±8000<br>±2000<br><br>±750<br>±500 | V | (6) |

Notes:

2. Concerned input pins are: CONF[0:1], RSTB, SI, SCLK, Clock, and CSB.
3. Concerned output pins are: CSNS, SYNC, and FSB.
4. Output current rating valid as long as maximum junction temperature is not exceeded. For computation of the maximum allowable output current, the thermal resistance of the package and the underlying heatsink must be taken into account.
5. Single pulse energy dissipation, single-pulse short-circuit method ($L_L$ = 0.5 mH, R = 48 mΩ $V_{PWR}$ = 28 V, $T_J$ = 150 °C initial).
6. ESD testing is performed in accordance with the Human body model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), and the charge device model (CDM), robotic ($C_{ZAP}$ = 4.0 pF).

**Table 3. Maximum ratings** ***(continued)***

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

| Symbol | Parameter | Maximum ratings | Unit | Notes |
|---|---|---|---|---|
| **Thermal ratings** | | | | |
| $T_A$<br>$T_J$ | Operating temperature<br>• Ambient<br>• Junction | <br>-40 to 125<br>-40 to 150 | °C | |
| $T_{STG}$ | Storage temperature | -55 to 150 | °C | |
| $R_{\theta JC}$ | Thermal resistance junction to case (exposed pad) | 1.4 | °C/W | |
| $R_{\theta JA}$ | Thermal resistance junction to ambient | 22 | °C/W | (7) |
| $T_{PPRT}$ | Peak package reflow temperature during reflow | Note 9 | °C | (8),(9) |

Notes:

7. Four layer board (2s2p), per JEDEC JESD51-6 with the board (JESD51-7) horizontal
8. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes), enter the core ID to view all orderable parts, and review parametrics.

## 4.2 Static electrical characteristics

**Table 4. Static electrical characteristics**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C, $V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Supply electrical characteristics** | | | | | | |
| $V_{PWR}$ | Supply voltage range:<br>• Full specification compliant<br>• Extended mode | <br>8.0<br>6.0 | <br>24<br>– | <br>36<br>58 | V | (10) |
| $I_{PWR(ON)}$ | $V_{PWR}$ supply current, device in Wake-up mode, channel On, open load outputs in ON-state, HS[0:1] open, IN[0:1] > $V_{IH}$ | – | 6.5 | 8.5 | mA | |
| $I_{PWR(SBY)}$ | $V_{PWR}$ supply current, device in Wake-up mode (Standby), channel Off open load in OFF-state detection disabled, HS[0:1] shorted to ground with $V_{DD}$ = 5.5 V and RSTB > $V_{WAKE}$ | – | 6.5 | 8.5 | mA | |
| $I_{PWR(SLEEP)}$ | Sleep state supply current<br>$V_{PWR}$ = 24 V, RSTB = IN[0:1] < $V_{WAKE}$, HS[0:1] connected to ground<br>• $T_A$ = 25 °C<br>• $T_A$ = 125 °C | <br><br>–<br>– | <br><br>3.0<br>– | <br><br>10.0<br>60.0 | µA | |
| $V_{DD(ON)}$ | $V_{DD}$ supply voltage | 3.0 | – | 5.5 | V | |
| $I_{DD(ON)}$ | $V_{DD}$ supply current at $V_{DD}$ = 5.5 V<br>• No SPI communication<br>• 8.0 MHz SPI communication | <br>–<br>– | <br>–<br>5.0 | <br>2.2<br>– | mA | (11) |
| $I_{DD(SLEEP)}$ | $V_{DD}$ sleep state current at $V_{DD}$ = 5.5 V with or without $V_{PWR}$ | – | – | 5.0 | µA | |
| $V_{PWR(OV)}$ | Overvoltage shutdown threshold | 39 | 42 | 45.5 | V | |
| $V_{PWR(OVHYS)}$ | Overvoltage shutdown hysteresis | 0.2 | 0.8 | 1.5 | V | |
| $V_{PWR(UV)}$ | Undervoltage shutdown threshold | 5.0 | – | 6.0 | V | (12) |
| $V_{PWR(POR)}$ | $V_{PWR}$ Power-on reset (POR) voltage threshold | 2.2 | 2.6 | 4.0 | V | (12) |
| $V_{DD(POR)}$ | $V_{DD}$ Power-on reset (POR) voltage threshold | 1.5 | 2.0 | 2.5 | V | (12) |
| $V_{DD(FAIL)}$ | $V_{DD}$ supply failure voltage threshold (assumed $V_{PWR}$ > $V_{PWR(UV)}$) | 2.2 | 2.5 | 2.8 | V | |
| $R_{DS(on)25}$ | ON-Resistance, Drain-to-Source ($I_{HS}$ = 1.0 A, $T_J$ = 25 °C) CSNS_ratio = 0<br>• $V_{PWR}$ = 8.0 V<br>• $V_{PWR}$ = 28 V<br>• $V_{PWR}$ = 36 V | <br>–<br>–<br>– | <br>18.7<br>18.7<br>18.7 | <br>–<br>–<br>– | mΩ | |

Notes

10. In Extended mode, availability of several device functions (channel control, value of $R_{DS(on)}$, overtemperature protection) is guaranteed, but compliance with the specified values in this document is not. Below 6.0 V, the device is only protected from overheating (thermal shutdown). Above $V_{PWR(OV)}$, the channels can only be turned ON when the overvoltage detection function has been disabled.
11. Typical value guaranteed per design.
12. When the device recovers from undervoltage and returns to Normal mode (6.0 V < $V_{PWR}$ < 58 V) before the end of the auto-retry period (see Auto-retry), the device performs normally. When $V_{PWR}$ drops below $V_{PWR(UV)}$, undervoltage is detected (see Undervoltage fault (Latchable fault) and EMC performances).

**Table 4. Static electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C, $V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Electrical characteristics of the output stage (HS0 and HS1)** | | | | | | |
| $R_{DS(on)150}$ | ON-Resistance, Drain-to-Source ($I_{HS}$ = 1.0 A,$T_J$ = 150 °C) CSNS_ratio = 0<br>• $V_{PWR}$ = 8.0 V<br>• $V_{PWR}$ = 28 V<br>• $V_{PWR}$ = 36 V | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>43<br>43<br>43 | mΩ | |
| $\Delta R_{DS(on)150}$ | ON-Resistance, Drain-to-Source difference from one channel to the other in Parallel mode ($I_{HS}$ = 1.0 A,$T_J$ = 150 °C) CSNS_ratio = X | -0.9 | – | 0.9 | mΩ | |
| $R_{SD(on)150}$ | ON-Resistance, Source-Drain ($I_{HS}$ = -1.0 A, $T_J$ = 150 °C, $V_{PWR}$ = -24 V) | – | – | 43 | mΩ | |
| $L_{SHORT}$ | Max. detectable wiring length (2.5 mm²) for severe short-circuit detection (see Severe short-circuit fault (Latchable fault)):<br>• High slew rate selected<br>• Medium slew rate selected<br>• Low slew rate selected | <br>30<br>55<br>110 | <br>100<br>175<br>365 | <br>180<br>300<br>620 | cm | |
| $I_{_OCH1_0}$<br>$I_{_OCH2_0}$<br>$I_{_OCM1_0}$<br>$I_{_OCM2_0}$<br>$I_{_OCL1_0}$<br>$I_{_OCL2_0}$<br>$I_{_OCL3_0}$ | Overcurrent detection thresholds with CSNS_ratio bit = 0 (CSR0) | 26.4<br>16.3<br>10.4<br>6.4<br>4.3<br>2.9<br>1.4 | 32<br>20.1<br>12.6<br>7.7<br>5.3<br>3.6<br>1.8 | 38.5<br>24.5<br>15.2<br>9.3<br>6.3<br>4.3<br>2.2 | A | |
| $I_{_OCH1_1}$<br>$I_{_OCH2_1}$<br>$I_{_OCM1_1}$<br>$I_{_OCM2_1}$<br>$I_{_OCL1_1}$<br>$I_{_OCL2_1}$<br>$I_{_OCL3_1}$ | Overcurrent detection thresholds with CSNS_ratio bit = 1(CSR1) | 8.9<br>5.6<br>3.5<br>2.2<br>1.45<br>0.98<br>0.48 | 10.7<br>6.8<br>4.25<br>2.7<br>1.75<br>1.2<br>0.6 | 12.8<br>8.2<br>5.1<br>3.2<br>2.1<br>1.45<br>0.72 | A | |
| $I_{OUT_LEAK}$ | Output (HS[x]) leakage current in sleep state (positive value = outgoing)<br>• $V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state)<br>$V_{HS,OFF}$ = $V_{PWR}$, device in sleep state ($V_{PWR}$ = 24 V)<br>$V_{HS,OFF}$ = $V_{PWR}$, device in sleep state ($V_{PWR}$ = 36 V) | <br>–<br>-120<br>-1400 | <br>–<br>–<br>– | <br>+5.0<br>+5.0<br>+5.0 | µA | |
| $I_{OUT_OFF}$ | Output biasing current in off-state (positive value = outgoing)<br>with OL_OFF disabled (worst case for $V_{PWR}$ = 36 V, $V_{HS,OFF}$ = 34 V)<br>• Fast slew rate selected<br>• Medium slew rate selected<br>• Slow slew rate selected<br>• With OL_OFF disabled and ECU ground disconnected ($V_{PWR}$ = 32 V) | <br>-620<br>-440<br>-330<br>0 | <br>-495<br>-360<br>-280<br>- | <br>-380<br>-280<br>-230<br>1000 | µA | |
| $V_{D_GND(CLAMP)}$ | Switch turn-on threshold for supply overvoltage ($V_{PWR}$ -GND) | 58 | – | 67 | V | |
| $V_{DS(CLAMP)}$ | Switch turn-on threshold for Drain-Source overvoltage (measured at $I_{OUT}$ = 500 mA | 58 | – | 66 | V | |
| $\Delta V_{DS(CLAMP)}$ | Switch turn-on threshold for Drain-Source overvoltage difference from one channel to the other in Parallel mode (at $I_{HS}$ = 500 mA) | -2.0 | – | +2.0 | V | |

**Table 4. Static electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C, $V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Electrical characteristics of the output stage (HS0 and HS1) (continued)** | | | | | | |
| $C_{SR0}$<br>$C_{SR1}$ | Current Sensing Ratio<br>• CSNS_ratio bit = 0 (high current mode)<br>• CSNS_ratio bit = 1 (low current mode) | <br>–<br>– | <br>1/1500<br>1/500 | <br>–<br>– | – | (13) |
| $I_{_LOAD_MIN}$ | Minimum measurable load current with compensated error | – | – | 50 | mA | (14) |
| $I_{CSR_LEAK}$ | CSNS leakage current in OFF state (CSNSx_en = 0, CSNS_ratio bit_x = 0) | -4.0 | – | +4.0 | µA | |
| $I_{_LOAD_ERR_SYS}$ | Systematic offset error (see Current sense errors) | – | -4.0 | – | mA | |
| $I_{_LOAD_ERR_RAND}$ | Random offset error | -125 | – | 125 | mA | |
| $I_{CSNS,MAX}$ | CSNS pin current sourcing capability, absolute upper limit | 5.15 | – | – | mA | |
| $E_{SR0_ERR}$ | $E_{SR0}$ output current sensing error (%), uncompensated at output current level (sense ratio $C_{SR0}$ selected):<br>$T_J$ = -40 °C<br>• 3.0 A<br>• 1.5 A<br>• 0.75 A<br>• 0.375 A<br>$T_J$ = 125 °C<br>• 3.0 A<br>• 1.5 A<br>• 0.75 A<br>• 0.375 A<br>$T_J$ = 25 °C to 125 °C<br>• 3.0 A<br>• 1.5 A<br>• 0.75 A<br>• 0.375 A | <br><br>-13<br>-12<br>-17<br>-26<br><br>-10<br>-9.0<br>-12<br>-15<br><br>-10<br>-10<br>-12<br>-16 | <br><br>–<br>–<br>–<br>–<br><br>–<br>–<br>–<br>–<br><br>–<br>–<br>–<br>– | <br><br>13<br>12<br>17<br>26<br><br>10<br>9.0<br>12<br>15<br><br>10<br>10<br>12<br>16 | % | (15) |

Notes:

13. Current sense ratio $C_{SRx} = I_{CSNS} / (I_{HS[x]} + I_{_LOAD_ERR_SYS})$
14. See note (15), but with $I_{CSNS_MEAS}$ obtained after compensation of $I_{_LOAD_ERR_RAND}$ (see Activation and use of offset compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration (see Application Note).
15. $E_{SRx_ERR} = (I_{CSNS_MEAS} / I_{CSNS_MODEL}) - 1$, with $I_{CSNS_MODEL} = (I(HS[x]) + I_{_LOAD_ERR_SYS}) * C_{SRx}$, ($I_{_LOAD_ERR_SYS}$ defined above, see section Current sense error model). With this model, load current becomes: $I(HS[x]) = I_{CSNS} / C_{SRx} - I_{_LOAD_ERR_SYS}$

**Table 4. Static electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C, $V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Electrical characteristics of the output stage (HS0 and HS1) (continued)** | | | | | | |
| $E_{SR0_ERR}$(Comp) | $E_{SR0}$ output current sensing error (%) after offset compensation at output current level (sense ratio $C_{SR0}$ selected):<br>$T_J$ = -40 °C<br>• 3.0 A<br>• 1.5 A<br>• 0.75 A<br>• 0.375 A<br>$T_J$ = 125 °C<br>• 3.0 A<br>• 1.5 A<br>• 0.75 A<br>• 0.375 A<br>$T_J$ = 25 °C to 125 °C<br>• 3.0 A<br>• 1.5 A<br>• 0.75 A<br>• 0.375 A | <br><br>-11<br>-11<br>-11<br>-11<br><br>-9.0<br>-9.0<br>-9.0<br>-10<br><br>-10<br>-9.0<br>-9.0<br>-10 | <br><br>–<br>–<br>–<br>–<br><br>–<br>–<br>–<br>–<br><br>–<br>–<br>–<br>– | <br><br>11<br>11<br>11<br>11<br><br>9.0<br>9.0<br>9.0<br>10<br><br>10<br>9.0<br>9.0<br>10 | % | (16) |
| $E_{SR1_ERR}$ | $E_{SR1}$ output current sensing error (%), uncompensated at output current level (sense ratio $C_{SR1}$ selected):<br>$T_J$ = -40 °C<br>• 0.75 A<br>$T_J$ = 125 °C<br>• 0.75 A<br>$T_J$ = 25 °C to 125 °C<br>• 0.75 A | <br><br>-16<br><br>-10<br><br>-12 | <br><br>–<br><br>–<br><br>– | <br><br>16<br><br>10<br><br>12 | % | (16) |
| $E_{SR1_ERR}$(Comp) | $E_{SR1}$ output current sensing error (%) after offset compensation at output current level (sense ratio $C_{SR1}$ selected):<br>$T_J$ = -40 °C<br>• 0.75 A<br>• 0.25 A<br>• 0.125 A<br>• 0.075 A<br>$T_J$ = 125 °C<br>• 0.75 A<br>• 0.25 A<br>• 0.125 A<br>• 0.075 A<br>$T_J$ = 25 °C to 125 °C<br>• 0.75 A<br>• 0.25 A<br>• 0.125 A<br>• 0.075 A | <br><br>-11<br>-14<br>-19<br>-29<br><br>-9.0<br>-10<br>-12<br>-16<br><br>-9.0<br>-11<br>-13<br>-21 | <br><br>–<br>–<br>–<br>–<br><br>–<br>–<br>–<br>–<br><br>–<br>–<br>–<br>– | <br><br>11<br>14<br>19<br>29<br><br>9.0<br>10<br>12<br>16<br><br>9.0<br>11<br>13<br>21 | % | (17) |

Notes:

16. $E_{SRx_ERR}$=($I_{CSNS_MEAS}$ / $I_{CSNS_MODEL}$) -1, with $I_{CSNS_MODEL}$ = (I(HS[x])+ $I_{_LOAD_ERR_SYS}$) * $C_{SRx}$ , ($I_{_LOAD_ERR_SYS}$ defined above, see section Current sense error model). With this model, load current becomes: I(HS[x]) = $I_{CSNS}$ / $C_{SRx}$ - $I_{_LOAD_ERR_SYS}$
17. See note (18), but with $I_{CSNS_MEAS}$ obtained after compensation of $I_{_LOAD_ERR_RAND}$ (see Activation and use of offset compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.

**Table 4. Static electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C, $V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Electrical characteristics of the output stage (HS0 and HS1) (continued)** | | | | | | |
| $E_{SR0_ERR_PAR}$ | $E_{SR0}$ output current sensing error in parallel mode (%), uncompensated) at outputs current level (sense ratio $C_{SR0}$ selected):<br>$T_J$ = -40 °C<br>• 6.0 A<br>• 3.0 A<br>$T_J$ = 125 °C<br>• 6.0 A<br>• 3.0 A<br>$T_J$ = 25 °C to 125 °C<br>• 6.0 A<br>• 3.0 A | <br><br>-10<br>-11<br><br>-8.0<br>-8.0<br><br>-9.0<br>-9.0 | <br><br>–<br>–<br><br>–<br>–<br><br>–<br>– | <br><br>10<br>11<br><br>8.0<br>8.0<br><br>9.0<br>9.0 | % | (18) |
| $V_{CL(CSNS)}$ | Current sense clamping voltage (condition: R(CSNS) > 10 kΩ) | 5.5 | – | 7.5 | V | |
| $I_{OLD(OFF)}$ | Open load detection current threshold in OFF state | 30 | – | 100 | µA | |
| $V_{OLD(THRES)}$ | Open load fault detection voltage threshold | 4.0 | – | 5.5 | V | |
| $I_{OLD(ON)}$ | Open load detection current threshold in ON state (see Open load detection in On state (OL_ON)):<br>• CSNS_ratio bit = 0<br>• CSNS_ratio bit = 1 (fast slew rate SR[1:0] = 10 mandatory for this function) | <br>40<br>4.0 | <br>150<br>7.0 | <br>300<br>10 | mA | |
| $t_{OLLED}$ | Time period of the periodically activated open load in ON state detection for CSNS_ratio bit = 1 | 105 | 150 | 195 | ms | |
| $V_{OSD(THRES)}$ | Output shorted-to-$V_{PWR}$ detection voltage threshold (channel in OFF state) | $V_{PWR}$-1.2 | $V_{PWR}$-0.8 | $V_{PWR}$-0.4 | V | |
| $V_{CL}$ | Switch turn-on threshold for negative output voltages (protects against negative transients) - (measured at $I_{OUT}$ = 100mA, channel in OFF state) | -38 | – | -32 | V | |
| $\Delta V_{CL}$ | Switch turn-on threshold for negative output voltages difference from one channel to the other in parallel mode - (measured at $I_{OUT}$ = 100 mA, channel in OFF state) | -2.0 | – | +2.0 | V | |
| $V_{HS_TH}$ | Switching State (On/Off) discrimination thresholds | 0.45*$V_{PWR}$ | 0.5*$V_{PWR}$ | 0.55*$V_{PWR}$ | V | |
| $T_{SD}$ | Shutdown temperature (power MOSFET junction; 6.0 V < $V_{PWR}$ < 58 V) | 160 | 175 | 190 | °C | |

Notes:

18. Minimum required value of open load impedance for detection of open load in OFF-state: 200 kΩ.($V_{OLD(THRES)}$ = $V_{HS}$ at $I_{OLD(OFF)}$)

**Table 4. Static electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C, $V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Electrical characteristics of the control interface pins** | | | | | | |
| $V_{IH}$ | Logic input voltage, high | 2.0 | – | 5.5 | V | (19) |
| $V_{IL}$ | Logic input voltage, low | -0.3 | – | 0.8 | V | (19) |
| $V_{WAKE}$ | Wake-up threshold voltage (IN[0:1] and RSTB) | 1.0 | – | 2.2 | V | (20) |
| $I_{DWN}$ | Internal pull-down current source (on inputs: CLOCK, SCLK and SI) | 5.0 | – | 20 | µA | (21) |
| $I_{UP_CSB}$ | Internal pull-up current source (input CSB) | 5.0 | – | 20 | µA | (22) |
| $I_{UP_CONF}$ | Internal pull-up current source (input CONF[0:1]) | 25 | – | 100 | µA | (23) |
| $C_{SO}$ | Capacitance of SO, FSB and FSOB pins in tri-state | – | – | 20 | pF | |
| $R_{DWN}$ | Internal pull-down resistance (RSTB and IN[0:1]) | 125 | 250 | 500 | kΩ | |
| $C_{IN}$ | Input capacitance | – | 4.0 | 12 | pF | (24) |
| $V_{SOH}$ | SO high-state output voltage<br>• ($I_{OH}$ = 1.0 mA) | $V_{DD}$-0.4 | – | – | V | |
| $V_{SOL}$ | SYNC, SO, FSOB and FSB low-state output voltage<br>• ($I_{OL}$ = -1.0 mA) | – | – | 0.4 | V | |
| $I_{SO(LEAK)}$ | SYNC, SO, CSNS, FSOB and FSB tri-state leakage current:<br>• 0.0 V < V(SO) < $V_{DD}$, or V(FS) or V(SYNC) = 5.5 V, or V(FSO) = 36 V or V(CSNS) = 0.0 V | -2.0 | 0.0 | 2.0 | µA | |
| $R_{CONF}$ | CONF[0:1]: Required values of the external pull-down resistor<br>• Lighting applications<br>• DC motor applications | <br>1.0<br>50 | <br>–<br>– | <br>10<br>Infinite | kΩ | |

Notes

19. High and low voltage ranges apply to SI, CSB, SCLK, RSTB, IN[0:1] and CLOCK input signals. The IN[0:1] signals may be derived from $V_{PWR}$ and can tolerate voltages up to 58 V.
20. Voltage above which the device wakes up
21. Valid for $V_{SI}$ ≥ 0.8 V and $V_{SCLK}$ ≥ 0.8 V and $V_{CLOCK}$ ≥ 0.8 V
22. Valid for $V_{CSB}$ ≤ 2.0 V. CSB has an internal pull-up current source derived from $V_{DD}$
23. Pins CONF[0:1] are connected to an internal current source, derived from an internal voltage regulator ($V_{REG}$ ~ 3.0 V).
24. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CONF[0:1], and CLOCK pins. This parameter is guaranteed by the manufacturing process but is not tested in production.

## 4.3 Dynamic electrical characteristics

**Table 5. Dynamic electrical characteristics**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C,$V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Output voltage switching characteristics** | | | | | | |
| $SR_{R_00}$<br>$SR_{F_00}$ | Rising and falling edges medium slew rate (SR[1:0] = 00)<br>• $V_{PWR}$ = 16 V<br>• $V_{PWR}$ = 28 V<br>• $V_{PWR}$ = 36 V | <br>0.4<br>0.6<br>0.7 | <br>–<br>–<br>– | <br>1.2<br>1.8<br>2.1 | V/µs | (25) |
| $SR_{R_01}$<br>$SR_{F_01}$ | Rising and falling edges low slew rate (SR[1:0] = 01)<br>• $V_{PWR}$ = 16 V<br>• $V_{PWR}$ = 28 V<br>• $V_{PWR}$ = 36 V | <br>0.2<br>0.3<br>0.35 | <br>–<br>–<br>– | <br>0.6<br>0.9<br>1.05 | V/µs | (25) |
| $SR_{R_10}$<br>$SR_{F_10}$ | Rising and falling edges high slew rate / SR[1:0] = 10)<br>• $V_{PWR}$ = 16 V<br>• $V_{PWR}$ = 28 V<br>• $V_{PWR}$ = 36 V | <br>0.8<br>1.2<br>1.4 | <br>–<br>–<br>– | <br>2.5<br>3.6<br>4.2 | V/µs | (25) |
| ΔSR | Rising/falling edge slew rate matching ($SR_R$ /$SR_F$)<br>• 16 V < $V_{PWR}$ < 36 V | 0.75 | – | 1.25 | | |
| ΔSR | Edge slew rate difference from one channel to the other in Parallel mode<br>16 V < $V_{PWR}$ < 36 V<br>SR[1:0] = 00<br>SR[1:0] = 01<br>SR[1:0] = 10 | <br><br>-0.16<br>-0.08<br>-0.32 | <br><br>0.0<br>0.0<br>0.0 | <br><br>0.16<br>0.08<br>0.32 | V/µs | (25) |
| $t_{DLY_00}$ | Output Turn-ON and Turn-OFF Delays (medium slew rate: SR[1:0] = 00)<br>• 16 V < $V_{PWR}$ < 36 V | 6.0 | – | 60 | µs | (26) |
| $t_{DLY_01}$ | Output Turn-ON and Turn-OFF delays (low slew rate / SR[1:0] = 01)<br>• 16 V < $V_{PWR}$ < 36 V | 10 | – | 120 | µs | (26) |
| $t_{DLY_10}$ | Output Turn-ON and Turn-OFF delays (high slew rate / SR[1:0] = 10)<br>• 16 V < $V_{PWR}$ < 36 V | 4.0 | – | 35 | µs | (26) |
| $\Delta t_{RF_00}$ | Turn-ON and Turn-OFF delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)<br>• $f_{PWM}$ = 400 Hz, 16 V < $V_{PWR}$ < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 00 | -25 | – | 25 | µs | |
| $\Delta t_{RF_01}$ | Turn-ON and Turn-OFF delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)<br>• $f_{PWM}$ = 200 Hz, 16 V < $V_{PWR}$ < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 01 | -50 | – | 50 | µs | |
| $\Delta t_{RF_10}$ | Turn-ON and Turn-OFF Delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$)<br>• $f_{PWM}$ = 1.0 kHz, 16 V < $V_{PWR}$ < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 10 | -13 | – | 13 | µs | |

Notes

25. Rising and falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Output voltage slew rate and delay).
26. Turn-ON delay time measured as delay between a rising edge of the channel control signal (IN[0:1] = 1) and the associated rising edge of the output voltage up to: $V_{HS[0:1]} = V_{PWR}$ / 2 (where $R_L$ = 25 Ω). Turn-OFF delay time is measured as time between a falling edge of the channel control signal (IN[0:1] = 0) and the associated falling edge of the output voltage up to the instant at which: $V_{HS[0:1]} = V_{PWR}$ / 2 ($R_L$ = 25 Ω)

**Table 5. Dynamic electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C,$V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Output voltage switching characteristics (continued)** | | | | | | |
| $\Delta t_{(DLY)}$ | Delay time difference from one channel to the other in Parallel mode<br>16 V < $V_{PWR}$ < 36 V<br>SR[1:0] = 00<br>SR[1:0] = 01<br>SR[1:0] = 10 | <br><br>-25<br>-50<br>-12 | <br><br>0.0<br>0.0<br>0.0 | <br><br>25<br>50<br>12 | µs | (27) |
| $t_{FAULT}$ | Fault detection delay time | – | 5.0 | 8.0 | µs | (28) |
| $t_{DETECT}$ | Output shutdown delay time | – | 10 | 15 | µs | (29) |
| $t_{CSNSVAL_00}$ | Current sense output settling time for SR[1:0] = 00 (medium slew rate)<br>• 16 V < $V_{PWR}$ < 36 V | 0.0 | – | 200 | µs | (30) |
| $t_{CSNSVAL_01}$ | Current sense output settling time for SR[1:0] = 01(low slew rate)<br>• 16 V < $V_{PWR}$ < 36 V | 0.0 | – | 315 | µs | (30) |
| $t_{CSNSVAL_10}$ | Current sense output settling time for SR[1:0] = 10 (high slew rate)<br>• 16 V < $V_{PWR}$ < 36 V | 0.0 | – | 165 | µs | (30) |
| $t_{SYNCVAL_00}$ | SYNC output signal delay for SR[1:0] = 00 (medium SR) | 20 | – | 120 | µs | (30) |
| $t_{SYNCVAL_01}$ | SYNC output signal delay for SR[1:0] = 01 (low SR) | 40 | – | 240 | µs | (30) |
| $t_{SYNCVAL_10}$ | SYNC output signal delay for SR[1:0] = 10 (high SR) | 10 | – | 60 | µs | (30) |
| $t_{SYNREAD_00}$ | Recommended sync_to_read delay SR[1:0] = 00 (medium slew rate) | 0.0 | – | 150 | µs | (30) |
| $t_{SYNREAD_01}$ | Recommended sync_to_read delay SR[1:0] = 01 (low slew rate) | 0.0 | – | 150 | µs | (30) |
| $t_{SYNREAD_10}$ | Recommended sync_to_read delay SR[1:0] = 10 (high slew rate) | 0.0 | – | 150 | µs | (30) |
| $t_{OCH1}$<br>$t_{OCH2}$ | Upper overcurrent threshold duration | 6.0<br>12.0 | 8.6<br>17.2 | 11.2<br>22.4 | ms | |
| $t_{OCM1_L}$<br>$t_{OCM2_L}$ | Medium overcurrent threshold duration (CONF = 0; Lighting profile) | 48<br>96 | 67<br>137 | 87<br>178 | ms | |
| $t_{OCM1_M}$<br>$t_{OCM2_M}$ | Medium overcurrent threshold duration (CONF = 1; DC motor profile) | 96<br>245 | 137<br>350 | 178<br>455 | ms | |

Notes

27. Rising and falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Output voltage slew rate and delay).
28. Time required to detect and report the fault to the FSB pin.
29. Time required to switch off the channel after detection of overtemperature (OT), overcurrent (OC), SC or UV error (time measured between start of the negative edge on the FSB pin and the falling edge on the output voltage until V(HS[0:1)) = 50% of $V_{PWR}$
30. Settling time ( = $t_{CSNSVAL_XX}$), SYNC output signal delay ( = $t_{SYNCVAL_XX}$) and Read-out delay ( = $t_{SYNREAD_XX}$) are defined for a stepped load current (100 mA< I(LOAD)<IOCLx A FOR CSNS_RATIO_S = 1, AND 300 mA< I(LOAD)<IOCLx A_0 FOR CSNS_RATIO_S = 0). See Figure 9 and Output current monitoring (CSNS).

**Table 5. Dynamic electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C,$V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Frequency and PWM duty cycle ranges** (protections fully operational, see Protective functions) (31) | | | | | | |
| $f_{CONTROL}$ | Switching frequency range - direct inputs | 0.0 | – | 1000 | Hz | |
| $f_{PWM_EXT}$ | Switching frequency range - external clock with internal PWM (recommended) | 20 | – | 1000 | Hz | |
| $f_{PWM_INT}$ | Switching frequency range - internal clock with internal PWM (recommended) | 60 | – | 1000 | Hz | |
| $R_{CONTROL}$ | Duty cycle range | 0.0 | – | 100 | % | |
| **Availability diagnostic functions for CSR0 over duty cycle and switching frequency (protections and diagnostics both fully operational, see Diagnostic features for the exact boundary values)** | | | | | | |
| $R_{PWM_1K_H}$ | Available duty cycle range, $f_{PWM}$ = 1.0 kHz high slew rate, PWM mode<br>• OL_OFF<br>• OL_ON<br>• OS | <br>0.0<br>35<br>0.0 | <br>–<br>–<br>– | <br>62<br>100<br>90 | % | (32) |
| $R_{PWM_400_M}$ | Available duty cycle range, $f_{PWM}$ = 400 Hz, medium slew rate, PWM mode<br>• OL_OFF<br>• OL_ON<br>• OS | <br>0.0<br>21<br>0.0 | <br>–<br>–<br>– | <br>81<br>100<br>88 | % | (32) |
| $R_{PWM_400_H}$ | Available duty cycle range, $f_{PWM}$ = 400 Hz, high slew rate, PWM mode<br>• OL_OFF<br>• OL_ON<br>• OS | <br>0.0<br>14<br>0.0 | <br>–<br>–<br>– | <br>84<br>100<br>95 | % | (32) |
| $R_{PWM_200_L}$ | Available duty cycle range, $f_{PWM}$ = 200 Hz, low slew rate mode, PWM mode<br>• OL_OFF<br>• OL_ON<br>• OS | <br>0.0<br>15<br>0.0 | <br>–<br>–<br>– | <br>86<br>100<br>93 | % | (32) |
| $R_{PWM_200_M}$ | Available duty cycle range, $f_{PWM}$ = 200 Hz, medium slew rate, PWM mode<br>• OL_OFF<br>• OL_ON<br>• OS | <br>0.0<br>11<br>0.0 | <br>–<br>–<br>– | <br>90<br>100<br>94 | % | (32) |
| $R_{PWM_100_L}$ | Available duty cycle range, $f_{PWM}$ = 100 Hz in low slew rate, PWM mode<br>• OL_OFF<br>• OL_ON<br>• OS | <br>0.0<br>8.0<br>0.0 | <br>–<br>–<br>– | <br>93<br>100<br>96 | % | (32) |
| $A_{FPWM(CAL)}$ | Deviation of the internal clock PWM frequency after calibration | -10 | – | +10 | % | (33) |
| $f_{PWM(0)}$ | Default output frequency when using an uncalibrated oscillator | 280 | 400 | 520 | Hz | |

Notes

31. In Direct input mode, the lower frequency limit is 0 Hz with RSTB=5.0 V and 4.0 Hz with RSTB = 0.0 V. Duty Cycle applies to instants at which $V_{HS}$ = 50 % $V_{PWR}$. For low duty cycle values, the effective value also depends on the value of the selected slew rate.
32. The device can be operated outside the specified duty cycle and frequency ranges (basic protective functions OC, SC, UV, OV, OT remain active) but the availability of the diagnostic functions OL_ON, OL_OFF, OS is affected.
33. Values guaranteed from 60 Hz to 1.0 kHz (recommended switching frequency range for internal clock operation).

**Table 5. Dynamic electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C,$V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Availability diagnostic functions over duty cycle and switching frequency (Continued) (protections & diagnostics both fully operational, see Diagnostic features for the exact boundary values)** | | | | | | |
| $t_{CSB(MIN)}$ | Minimal required low time during calibration of the internal clock through CSB | 1.0 | 1.5 | 2.0 | µs | |
| $t_{CSB(MAX)}$ | Maximal allowed low time during calibration of the internal clock through CSB | 70 | 100 | 130 | µs | |
| $f_{CLOCK}$ | Recommended external clock frequency range (external clock/PWM Module) | 15 | – | 512 | kHz | |
| $f_{CLOCK(MAX)}$ | Upper detection threshold for external clock frequency monitoring | 512 | 730 | 930 | kHz | |
| $f_{CLOCK(MIN)}$ | Lower detection threshold for external clock frequency monitoring | 5.0 | 7.0 | 10 | kHz | |
| **Timing: SPI port, IN[0]/ IN[1] signals and autoretry** | | | | | | |
| $t_{IN}$ | Required low time allowing delatching or triggering Sleep mode (Direct input mode) | 175 | 250 | 325 | ms | |
| $t_{WDTO}$ | Watchdog timeout for entering Fail-safe mode due to loss of SPI contact | 217 | 310 | 400 | ms | (34) |
| $t_{AUTO_00}$<br>$t_{AUTO_01}$<br>$t_{AUTO_10}$<br>$t_{AUTO_11}$ | Auto-Retry repetition period (when activated):<br>• Auto_period bits = 00<br>• Auto_period bits = 01<br>• Auto_period bits = 10<br>• Auto_period bits = 11 | <br>105<br>52.5<br>26.2<br>13.1 | <br>150<br>75<br>7.5<br>17.7 | <br>195<br>97.5<br>47.8<br>24.4 | ms | |
| **GND pin temperature sensing function** | | | | | | |
| $T_{OTWAR}$ | Thermal prewarning detection threshold | 110 | 125 | 140 | °C | (35) |
| $T_{FEED}$ | Temperature sensing output voltage at $T_A$ = 25 °C (470 Ω < $R_{CSNS}$ < 10 kΩ) | 918 | 1078 | 1238 | mV | |
| $DT_{FEED}$ | Gain temperature sensing output at $T_A$ = 25 °C (470 Ω < $R_{CSNS}$ < 10 kΩ) | 10.7 | 11.1 | 11.5 | mV/°C | (35) |
| $T_{FEED_ERROR}$ | Temperature sensing error, range [-40 °C, 150 °C], default | -15 | – | +15 | °C | (35) |
| $T_{FEED_ERROR_CAL}$ | Temperature sensing error, [-40 °C, 150 °C] after 1 point calibration at 25 °C | -5.0 | – | +5.0 | °C | (35) |

Notes

34. Only when the WD_dis bit set to logic [0] (default). Watchdog timeout defined from the rising edge on RST to rising edge HS[0,1]
35. Values were obtained by lab. characterization
36. Parameters guaranteed by design. It is recommended to tie unused SPI-pins to GND by resistors 1.0 k <R <10 k.

**Table 5. Dynamic electrical characteristics (continued)**

Unless specified otherwise: 8.0 V ≤ $V_{PWR}$ ≤ 36 V, 3.0 V ≤ $V_{DD}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions $T_A$ = 25 °C,$V_{PWR}$ = 28 V and $V_{DD}$ = 5.0 V, unless specified otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **SPI interface electrical characteristics** (36) | | | | | | |
| $f_{SPI}$ | Maximum operating frequency of the Serial Peripheral Interface (SPI) | – | – | 8.0 | MHz | (42) |
| $t_{WRSTB}$ | Required low-state duration for reset RSTB | 10 | – | – | µs | (37) |
| $t_{CSB}$ | Required duration from the rising to the falling edge of CSB (required setup time) | 1.0 | – | – | µs | (38) |
| $t_{ENBL}$ | Rising edge of RSTB to falling edge of CSB (required setup time) | 5.0 | – | – | µs | (38) |
| $t_{LEAD}$ | Falling edge of CSB to rising edge of SCLK (required setup time) | 500 | – | – | ns | (38) |
| $t_{LAG}$ | Falling edge of SCLK to rising edge of CSB (required setup lag time) | 60 | – | – | ns | (38) |
| $t_{WSCLKh}$ | Required high state duration of SCLK (required setup time) | 50 | – | – | ns | (38) |
| $t_{WSCLKl}$ | Required low state duration of SCLK (required setup time) | 50 | – | – | ns | (38) |
| $t_{SI(SU)}$ | SI to falling edge of SCLK (required setup time) | 15 | – | – | ns | (39) |
| $t_{SI(H)}$ | Falling edge of SCLK to SI (required hold time of the SI signal) | 30 | – | – | ns | (39) |
| $t_{RSO}$ | SO rise time<br>• $C_L$ = 80 pF | – | – | 20 | ns | |
| $t_{FSO}$ | SO fall time<br>• $C_L$ = 80 pF | – | – | 20 | ns | |
| $t_{RSI}$ | SI, CSB, SCLK, Max. Rise Time allowing operation at $f_{SPI}$ = 8.0 MHz | – | – | 11 | ns | (39) |
| $t_{FSI}$ | SI, CSB, SCLK, Max. Fall Time allowing operation at $f_{SPI}$ = 8.0 MHz | – | – | 11 | ns | (39) |
| $t_{VALID}$ | Time from rising edge of SCLK to reach a valid level at the SO pin | – | – | 44 | ns | (40) |
| $t_{SOEN}$ | Time from falling edge of CSB to reach low-impedance on SO (access time) | – | – | 30 | ns | (41) |

Notes:

37. RSTB low duration is defined as the minimum time required to switch off the channel when previously put ON in SPI mode (direct inputs inactive).
38. Minimum setup time required for the device is the minimum required time that the microcontroller must wait or remain in a given state.
39. Rise and Fall time of incoming SI, CSB, and SCLK signals.
40. Time required for output data to be available for use at SO, measured with a 1.0 kΩ series resistor connected CSB.
41. Time required for output data to be terminated at SO measured with a 1.0 kΩ series resistor connected CSB.
42. For clock frequencies > 4.0 MHz, series resistors on the SPI pins should preferably be removed. Otherwise, 470 pF ($V_{MAX.}$ > 40 V) ceramic speed-up capacitors in parallel with the >8.0 kΩ input resistors are required on pins SCLK, SI, SO, CS

## 4.4 Timing diagrams

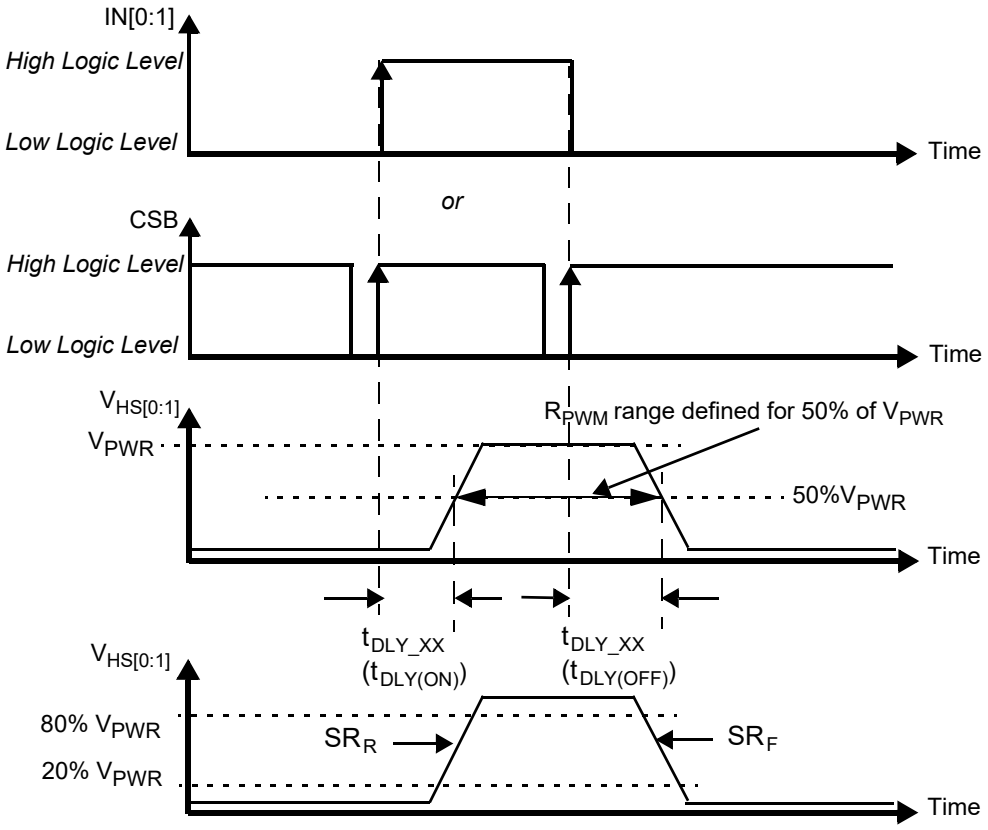



**Figure 4. Output voltage slew rate and delay**

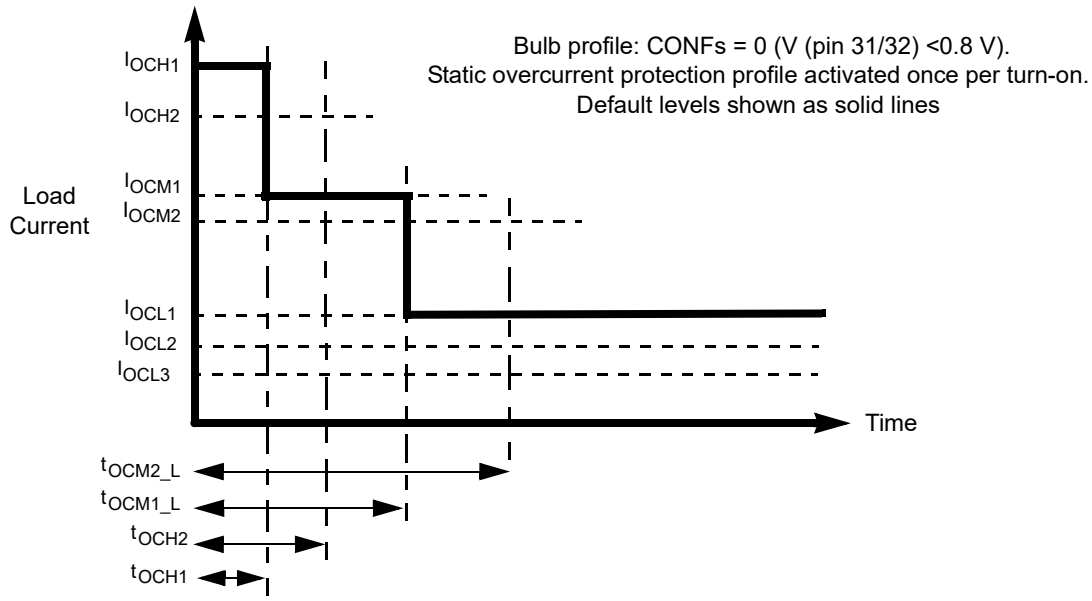



**Figure 5. Overcurrent protection profile for bulb applications**

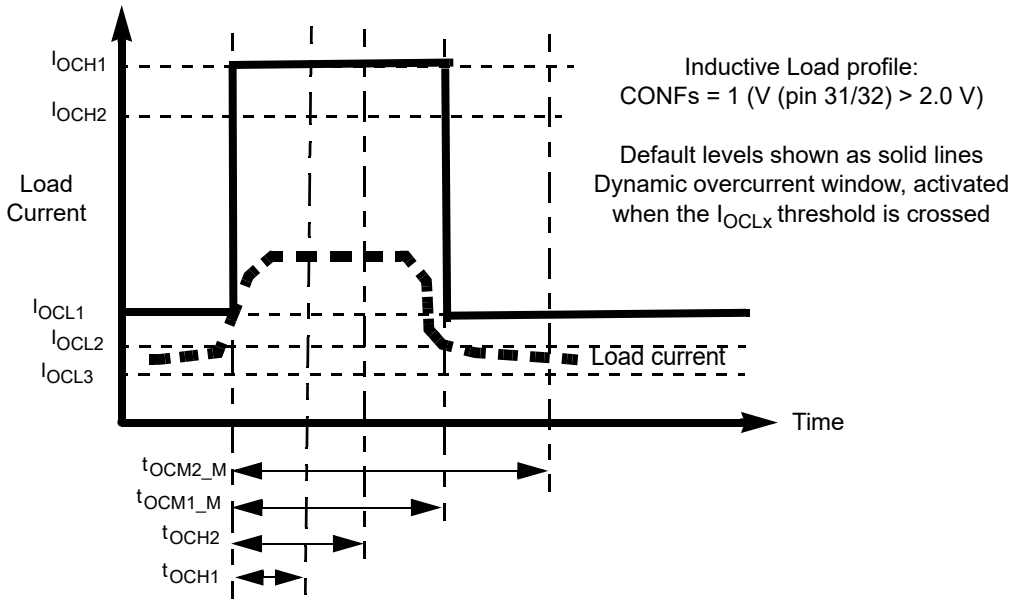



**Figure 6. Overcurrent protection profile for applications with inductive loads (DC motors, solenoids)**

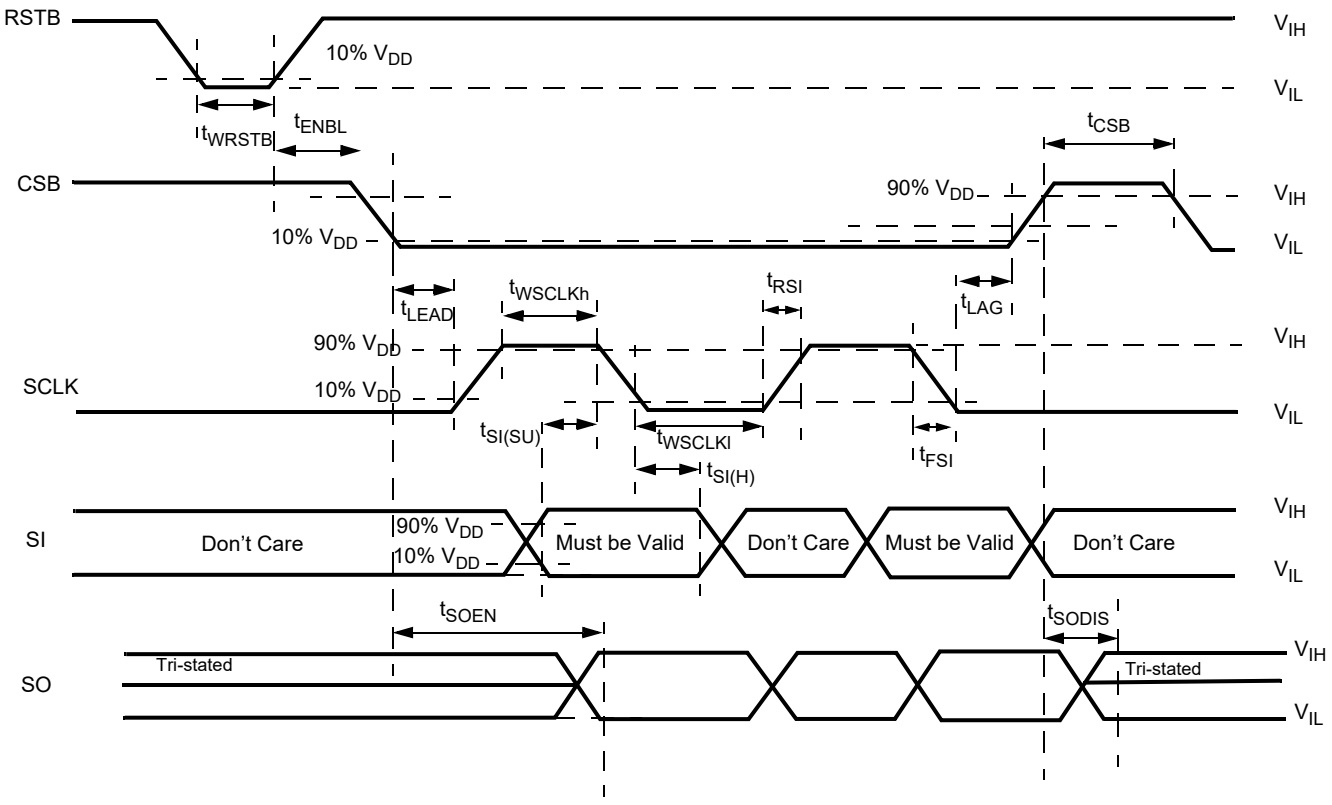



**Figure 7. Timing requirements during SPI communication**

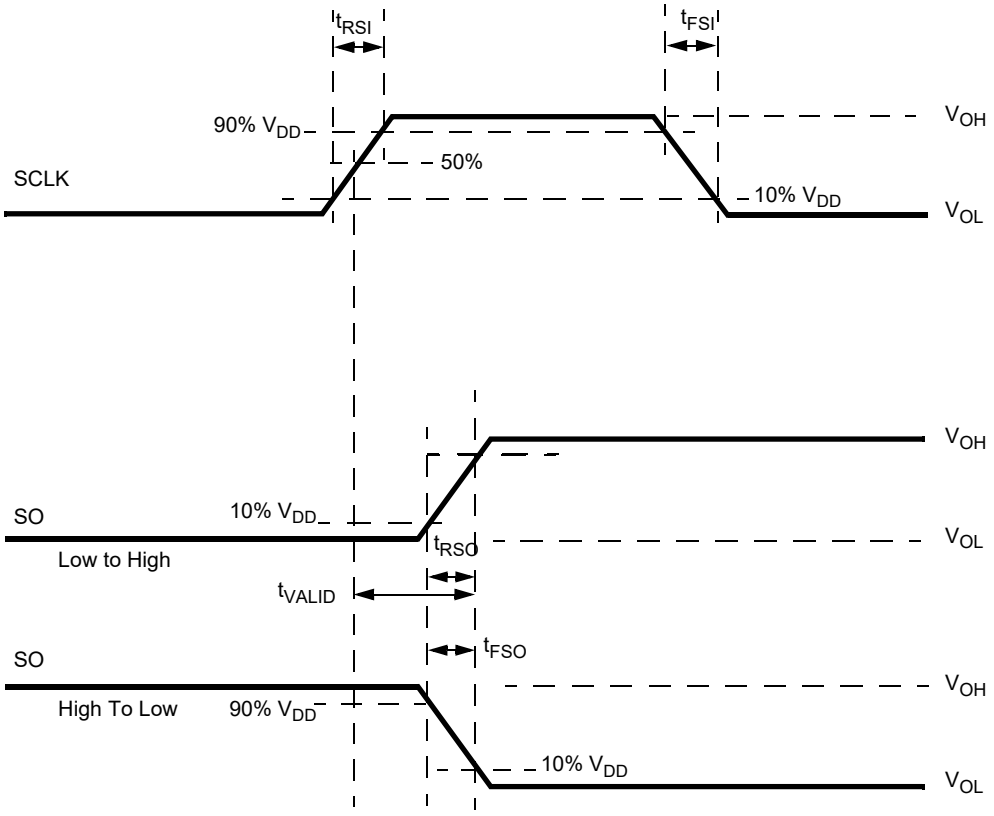



**Figure 8. Timing diagram for serial output (SO) data communication**

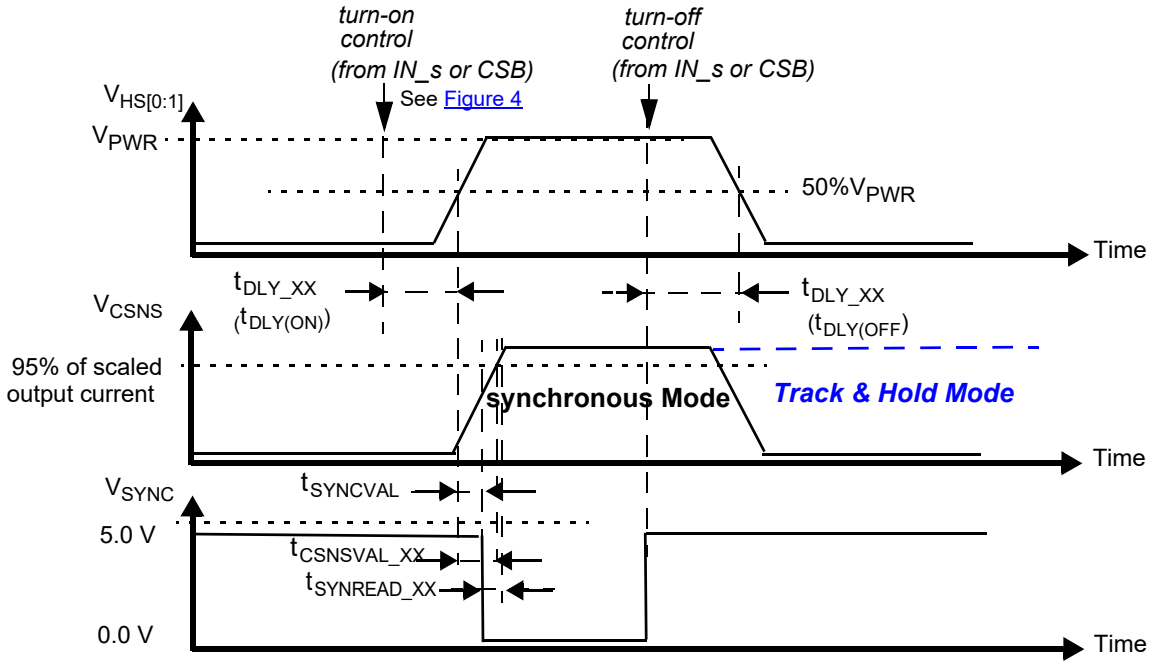



**Figure 9. Synchronous and track-and-hold current sensing modes: associated delay and settling time**

# 5 Functional description

## 5.1 Introduction

The 22XS4200 is a two-channel, 24 V high-side switch with integrated control and diagnostics designed for truck and bus applications. The device provides a high number of protective functions. Both low $R_{DS(on)}$ channels (<22 mΩ) can independently drive various load types like light bulbs, solenoid actuators, or DC motors. Device control and diagnostics are configured through a 16-bit SPI port with daisy chain capability.

Independently programmable output voltage slew rates allow satisfying electromagnetic compatibility (EMC) requirements. Both channels can independently be operated in three different switching modes: internal clock and internal PWM mode (fully autonomous operation), external clock and internal PWM mode, and direct control switching mode.

Current sensing with an adjustable ratio is available on both channels, allowing both high current (bulbs) and low current (LED) monitoring. By activating the Track & Hold mode, current monitoring can be performed during the switch-Off phase. This allows random access to the current sense functionality. A patented offset compensation technique further enhances current sense accuracy.

To avoid turning off upon inrush current, while being able to monitor it, the device features a dynamic overcurrent threshold profile. For bulbs, this profile is a stair function with stages of which the height and width are programmable through the SPI port. DC motors can be protected from overheating by activating a specific window-shaped overcurrent profile that allow stall currents of limited duration.

Whenever communication with the external micro-controller is lost, the device enters Fail-safe operation mode, but remains operational, controllable, and protected.

## 5.2 Pin assignment and functions

Functions and register bits that are implemented independently for both channels have extension "_s". Maximum ratings of the pins are given in Table 3.

### 5.2.1 Output current monitoring (CSNS)

The CS pin allows independent current monitoring of channel 0 or channel 1 up to the steady-state overcurrent threshold. It can also be used to sense the device temperature. The different functions are selected by setting bits CSNS1_en and CSNS0_en to the appropriate value (Table 23). When the CSNS pin is sensed during switch-off in the (optional) Track & Hold mode (see Figure 9), it outputs the scaled value of the load current as it was just before turn-Off. When several devices share the same pull-down resistor, the CSNS pins of devices the current of which is not monitored must be tri-stated. This is accomplished by setting CSNS0_en = 0 and CSNS1_en = 0 in the GCR register (Table 10). Settling time ($t_{CSNSVAL_XX}$) is defined as the time between the instant at the middle of the output voltage's rising edge (HS[0:1] = 50% of $V_{PWR}$), and the instant at which the voltage on the CSNS-pin has settled to ±5.0% of its final value. Anytime an overcurrent window is active, the CSNS pin is disabled (see Overcurrent detection on resistive and inductive loads). The current and temperature sensing functions are unavailable in Fail-safe mode and in Normal mode when operating without the $V_{DD}$ supply voltage. In order to generate a voltage output, a pull-down resistor is required (R(CSNS)=1.0 kΩ typ. and 470 < R(CSNS) < 10 k). When the current sense resistor connected to the CSNS pin is disconnected, the CSNS voltage is clamped to $V_{CL(CSNS)}$. The CSNS pin can source currents up to about 5.6 mA.

### 5.2.2 Current sense synchronization (SYNC)

To synchronize current sensing with an external process, the SYNC signal can be connected to a digital input of an external MCU. SYNC is asserted logic low when the current sense signal is accurate and ready to be read. The current sense signal on the CSNS pin has the specified accuracy $t_{SYNREAD_XX}$ seconds after the falling edge on the SYNC pin (Figure 9) and remains valid until a rising edge is generated. The rising edge that is generated by the SYNC pin at the turn-OFF instant (internal or external) may also be used to implement synchronization with the external MCU. Parameter $t_{SYNCVAL_XX}$ is defined as the time between the instant at the middle of the output-voltage rising edge (HS[0:1] = 50% of VPWR), and the instant at which the voltage on the SYNC-pin drops below 0.4 V ($V_{SOL}$). The SYNC pins of different devices can be connected together to save µ-controller input channels. However, in this configuration, the CSNS function of only one device should be active at a time. Otherwise, the MCU does not determine the origin of the SYNC signal. The SYNC pin is open drain and requires an external pull-up resistor to VDD.

### 5.2.3 Direct control inputs (IN0 and IN1)

The IN[0:1] pins allow direct control of both channels. A logic [0] level turns off the channel and a logic[1] level turns it on (Channel control in Normal mode). When the device is in Sleep mode, a transition from logic 0 to logic 1 on any of these pins wake it up (Sleep mode). If it is desired to automatically turn on the channels after a transition to Fail-safe mode, inputs IN[0] and IN[1] must be externally connected to the VPWR pin by a pull-up resistor (e.g. 10 kΩ typ.). However, this prevents the device from going into Sleep mode. Both IN pins are internally connected to a pull-down resistor.

### 5.2.4 Configuration inputs (CONF0 and CONF1)

The CONF[0:1] input pins allow configuring both channels for the appropriate load type. CONF = 0 activates the bulb overcurrent protection profile, and CONF = 1 the DC motor profile. These inputs are connected to an internal voltage regulator of 3.3 V by an internal pull-up current source $I_{UP}$. Therefore, CONF = 1 is the default value when these pins are disconnected. Details on how to configure the channels are given in Table 9.

### 5.2.5 Fault status (FSB)

This open drain output is asserted low when any of the following faults occurs (see Fault mode): overcurrent (OC), overtemperature (OT), Output connected to $V_{PWR}$, Severe short-circuit (SC), open load in ON state (OL_ON), open load in OFF state (OL_OFF), External Clock-fail (CLOCK_fail), overvoltage (OV), undervoltage (UV). Each fault type has its own assigned bit inside the STATR, FAULTR_s, or DIAGR_s register. Fault type identification and fault bit reset are accomplished by reading out these registers. They are part of the SO register (Fault mode) and are accessed through the SPI port.

### 5.2.6 PWM clock (CLOCK)

This pin is the input for an external clock signal that controls the internal PWM module.The clock signal is monitored by the device. The PWM module controls ON-time and turn-ON delay of the selected channels. The CLOCK pin should not be confused with the SCLK pin, which is the clock pin of the SPI interface. CLOCK has an internal pull-down current source ($I_{DWN}$) to GND.

### 5.2.7 Reset (RSTB)

All SPI register contents are reset when RSTB = 0. When RSTB = 0, the device returns to Sleep mode $t_{IN}$ sec. after the last falling edge of the last active IN[0:1] signal. As long as the Reset input (RSTB pin) is at logic 0 and both direct input states are low, the device remains in Sleep mode (Channel configuration through the SPI). A 0-to-1 transition on RSTB wakes up the device and starts a watchdog timer to check the continuous presence of the SPI signals. To do this, the device monitors the contents of the first bit (WDIN bit) of all SPI words following that transition (regardless the register it is contained in). When this contents is not alternated within a duration $t_{WDTO}$, SPI communication is considered lost, and Fail-safe mode is entered (Entering fail-safe mode). RSTB is internally pulled-down to GND by resistor $R_{DWN}$.

### 5.2.8 Chip select (CSB)

Data communication over the SPI port is enabled when the CSB pin is in the logic [0] state. Data from the Input Shift registers are locked in the addressed SI registers on the rising edge of CSB. The device transfers the contents of one of the eight internal registers to the SO register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is at logic [0] (Figure 7 and Figure 8). CSB is internally pulled up to $V_{DD}$ through $I_{UP}$.

### 5.2.9 SPI serial clock (SCLK)

The SCLK pin clocks the SPI data communication of the device. The serial input pin (SI) transfers data to the SI shift registers on the falling edge of the SCLK signal while data in the SO registers are transferred to the SO pin on the rising edge of the SCLK signal. The SCLK pin must be in low state when CSB makes any transition. For this reason, it is recommended to have the SCLK pin in the logic [0] state when the device is not accessed (CSB is at logic [1]). When CSB is set to logic [1], the signals at the SCLK and SI pins are ignored and the SO output is tri-stated (high-impedance). The SCLK pin is connected to an internal pull-down current source $I_{DWN}$.

### 5.2.10 Serial input (SI)

Serial input (SI) data bits are shifted in at this pin. SI data is read on the falling edge of SCLK. 16-bit data packages are required on the SI pin (see Figure 7), starting with bit D15 (MSB) and ending with D0 (LSB). All the internal device registers are addressed and controlled by a 4-bit address (D9-D12) described in Table 14. Register addresses and function attribution are described in Table 15. The SI pin is internally connected to a pull-down current source, $I_{DWN}$.

### 5.2.11 Supply of the digital circuitry (VDD)

This pin supplies the SPI circuit (3.3 V or 5.0 V). When lost, all circuitry becomes supplied by a $V_{PWR}$ derived voltage, except the SPI's SO shift-register that can no longer be read.

### 5.2.12 Ground (GND)

This is the GND pin common for both the SPI and the other circuitry.

### 5.2.13 Positive supply pin (VPWR)

This pin is the positive supply and the common input pin of both switches. A 100 nF ceramic capacitor must be connected between VPWR and GND, close to the device. In addition, it is recommended to put a ceramic capacitor of at least 1.0 µF in parallel with this 100 nF capacitor.

### 5.2.14 Serial output (SO)

The SO pin is a tri-stateable output pin that conveys data from one of the 13 internal SO registers or from the previous SI register to the outside world. The SO pin remains in a high-impedance state (tri-state) until the CSB pin becomes logic [0]. It then transfers the SPI data (device state, configuration, fault information). The SO pin changes state at the rising edge of the SCLK signal. For daisy-chaining, it can be read out on the falling edge of SCLK. $V_{DD}$ must be present before the SO registers can be read. The SO register assignment is described in Table 13.

### 5.2.15 Power switch output pins (HS0 and HS1)

HS0 and HS1 are the output pins of the power switches, to be connected to the loads. A ceramic capacitor (<= 22 nF (+/- 20%) is recommended between these pins and GND for optimal EMC performances.

### 5.2.16 Fail-safe output (FSOB)

This pin (active low) is used to indicate loss of SPI communication or loss of SPI supply voltage, $V_{DD.}$ This open drain output requires an external pull-up resistor to VPWR.

## 5.3 Functional internal block description

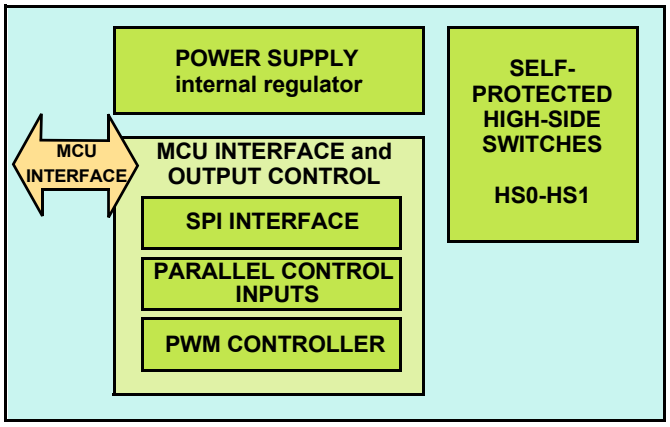



**Figure 10. Internal block description**

### 5.3.1 Power supply

The device operates with supply voltages from 6.0 V to 58 V ($V_{PWR}$), but is full spec. compliant between 8.0 V and 36 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VDD pin (5.0 V typ.) supplies the output register of the Serial Peripheral Interface (SPI). Consequently, the SPI registers cannot be read without presence of $V_{DD}$. The employed IC architecture guarantees a low quiescent current in Sleep mode.

### 5.3.2 Switch output pins HS0 and HS1

HS0 and HS1 are the output pins of the power switches. Both channels are protected against various kinds of short-circuits and have active clamp circuitry that may be activated when switching off inductive loads. Many protective and diagnostic functions are available. For large inductive loads, it is recommended to use a freewheeling diode. The device can be configured to control the output switches in parallel, which guarantees good switching synchronization.

### 5.3.3 Communication interface and device control

In Normal mode the output channels can either be controlled by the direct inputs or by the internal PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, $V_{DD}$ has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: open load, short-circuit to battery, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, undervoltage, and overvoltage. The SPI port can be supplied either by a 5.0 V or by a 3.3 V voltage supply. For direct input control, $V_{DD}$ is not required.

A pulse width modulation (PWM) circuit allows driving loads at frequencies up to 1.0 kHz from an external or an internal clock. SPI communication is required to set these options.

# 6 Functional device operation

## 6.1 Operation and operating modes

The device possesses two high-side switches (channels) each of which can be controlled independently. The device has four fundamental operating modes: Sleep, Normal, Fail-safe, and Fault mode, as shown in Table 6.

Each channel can be controlled in three different ways in Normal mode: by a signal on the Direct Input pin, by an internal clock signal (autonomous operation) or by an external clock signal. For bidirectional SPI communication, a second supply voltage is required ($V_{DD}$ = 5.0 V or 3.3 V). When only the direct inputs IN[x] are used, $V_{DD}$ is not required.

### 6.1.1 Device start-up sequence

To put the device in a known configuration and guarantee predictable behavior, the device must undergo a wake-up sequence. However, it should not be woken up earlier than the moment at which $V_{PWR}$ has exceeded its undervoltage threshold, $V_{PWR}$(UV), and $V_{DD}$ has exceeded its supply failure threshold, $V_{DD}$(FAIL). In applications using the SPI port, the device is typically put in wake mode by setting RSTB=1. Wake-up of applications with direct input control can be achieved by having signals IN_ON[0] = 1 or IN_ON[1 ]= 1 (see Figure 11). After wake-up, all SPI register contents are reset (as defined in Table 12 and Table 13) and Normal mode is entered. All the device functions are available 50 µs later (typically).

If the start-up sequence is not performed at device start-up, its configuration may be undetermined and correct operation is not guaranteed. In situations where the above described start-up sequence can not be performed, it is recommended to generate a wake-up event after the moment $V_{PWR}$ has reached the undervoltage threshold.

### 6.1.2 Channel configuration through the SPI

#### 6.1.2.1 Setting the channel configuration

The channel configuration is determined by the contents of the pulse-width (PWMR_s), the configuration (CONFR_s) and the overcurrent (OCR_s) registers. They allow setting, among others, the following parameters: duty cycle, delay, Slew Rate, PWM enable (PWM_en), clock selection (CLOCK_sel), prescaler (PR), and direct_input disable (DIR_dis). Extension "_s" means that these registers exist for each of both channels. Function assignment is described in detail in the section SI register addressing.

#### 6.1.2.2 Reading back the channel's status and settings

The channel's global switching and operating states (On/Off, normal/fault) are all contained in the SO-STATR register (see Table 16). The precise fault type can be found by reading out the FAULTR_s and STATR registers. The current channel settings (channel configuration) can be known by reading the PWMR, CONF, OCR, RETRYR, GCR, and DIAG registers (see section Serial output register assignment and beyond).

### 6.1.3 Normal mode

Normal mode (bit NM = 1) can be entered in two ways: either by driving the device through the direct inputs (IN[x]) or by establishing SPI communication (requires RSTB = high). Bidirectional SPI communication additionally requires the presence of $V_{DD}$. To maintain the device in Normal mode, communication must take place regularly (see Entering and maintaining Normal mode). The device is in Normal mode (NM) when:

- $V_{PWR}$ (and $V_{DD}$) are within the normal range and
- wake-up = 1, and
- fail-safe = 0, and
- fault = 0.

### 6.1.3.1 Channel control in Normal mode

In Direct input mode, the channel's switching state (On/Off) is controlled by the logic state of the direct input signal with the default values (00) of turn-on delay and slew rate, specified in Table 5. In internal clock mode, the switching state is controlled by an internal clock signal (Internal clock and internal PWM (Clock_int_s bit = 1)). Frequency, slew rate, duty cycle, and turn-on delay are programmable independently for both channels. In external clock mode, the frequency of the external clock controls the output's PWM frequency, but slew rate, duty cycle, and turn-on delay are still programmable.

### 6.1.3.2 Factors determining the channel's switching state

The switching state of a channel is defined by the instantaneous value of the output voltage. It is defined as "On" when the output voltage V(HS[x]) > $V_{PWR}$ /2 and "Off" when V(HS[x]) < $V_{PWR}$ /2. The channel's switching state should not be confused with the device's internal channel control state hson[x] (= High-side On). Signal hson[x] defines the targeted switching state of the channel (On/Off). It is either controlled by the value of the direct input signal or by the internal/external clock signals combined with the SPI register settings. The value of hson[x] is given by the following boolean expression:

hson[x] = [(IN[x] and $\overline{\text{DIR_dis[x]}}$) or (On bit [x] and Duty_cycle[x] and PWM_en[x] = 1) or (On bit [x] and PWM_en[x] = 0)].

**In this expression Duty_cycle[x] represents the value of the duty cycle, set by bits D7…D0 of the PWMR register (Table 7). The channel's actual switching state may differ from the control signal's state in the following cases:**

- short-circuits to GND, before automatic turn-Off (t < $t_{FAULT}$)
- short-circuits to $V_{PWR}$ when the channel is set to Off
- $V_{PWR}$ < 13 V when open load in Off-state detection is selected and the load is actually lost
- during the turn-on transition as long as V(HS[x])< $V_{PWR}$/2
- during the turn-off transition as long as V(HS[x]) > $V_{PWR}$/2

### 6.1.3.3 Entering and maintaining Normal mode

A 0-to-1 transition on RSTB, (when both $V_{PWR}$ and $V_{DD}$ are present) or on any of both direct inputs IN[x] (when only supplied by $V_{PWR}$) puts the device in Normal mode. If desired, the device can be operated in Normal mode without $V_{DD}$, but this requires that at least one of both direct inputs be regularly turned on (Operation and operating modes). To maintain the device in Normal mode (NM), communication must take place on a regular basis.

For SPI communication, the state of the WDIN bit must be alternated at least every 310 ms (typ.) ($t_{WDTO}$), unless the WD_disable bit is set to 1.

For direct input control, the timing requirements are shown in Figure 11. A signal called IN_ON[x] is not directly accessible to the user but is used by the internal logic circuitry to determine the device state. When no activity is detected on a direct input pin (IN[x]) for a time longer than $t_{IN}$ = 250 ms (typ.), timeout is detected and IN_ON[x] goes low. When this occurs on both channels, Sleep mode is entered (Sleep mode), provided reset = RSTB = 0.

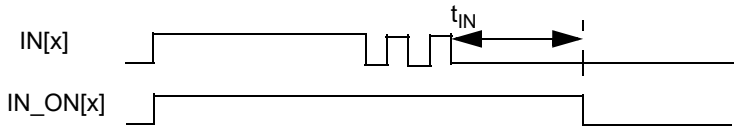



**Figure 11. Relation between signals IN(x) and IN_ON[x]**

### 6.1.3.4 Direct control mode

When RSTB = 0 (and also in Fail-safe mode), the channels are merely controlled by the direct input pins IN[x]. All protective functions (OC, OT, SC, OV, and UV) are operational including auto-retry. To avoid entering Sleep mode at frequencies < 4.0 Hz, reset should be set to RSTB = 1.

### 6.1.3.5 Going from Normal to Fail-safe, Fault or Sleep mode

The device changes from Normal to Fail-safe (Fail-safe mode), Sleep mode (Sleep mode), or Fault mode (Fault mode), according to the value of the following signals (see Table 6).

- wake-up = RSTB or IN_ON[0] or IN_ON[1]
- fail-safe = ($V_{DD}$ Failure and $V_{DD}$_FAIL_en) or (SPI watchdog timeout ($t_{WDTO}$) and WD_dis = 0)
- fault = OC[0:1] or OT[0:1] or SC[0:1] or UV or (OV and $\overline{OV_dis}$)

**Table 6. Device operating modes**

| Mode | Wake-up | Fail-safe | Fault | Comments |
|---|---|---|---|---|
| Sleep | 0 | x | x | All channels are OFF |
| Normal | 1 | 0 | 0 | The SPI Watchdog is active when: VDD = 5.0 V, WD_dis = 0, RSTB = 1 |
| Fail-safe | 1 | 1 | 0 | The channels are controlled by the IN inputs (see Fail-safe mode) |
| Fault | 1 | X | 1 | The channels are OFF, see Fault mode |

x = Don't care.

It enters Fail-safe mode in case of a timeout on SPI communication or when $V_{DD}$ is lost after having been initially present (if this function was previously enabled by setting: $V_{DD_FAIL_EN}$ bit = [1]). Setting watchdog disabled (WD_dis = 1, D4 of the GCR register) avoids entering Fail-safe mode after watchdog timeout. Device behavior upon fault occurrence is explained in the paragraph on Faults (Fault mode).

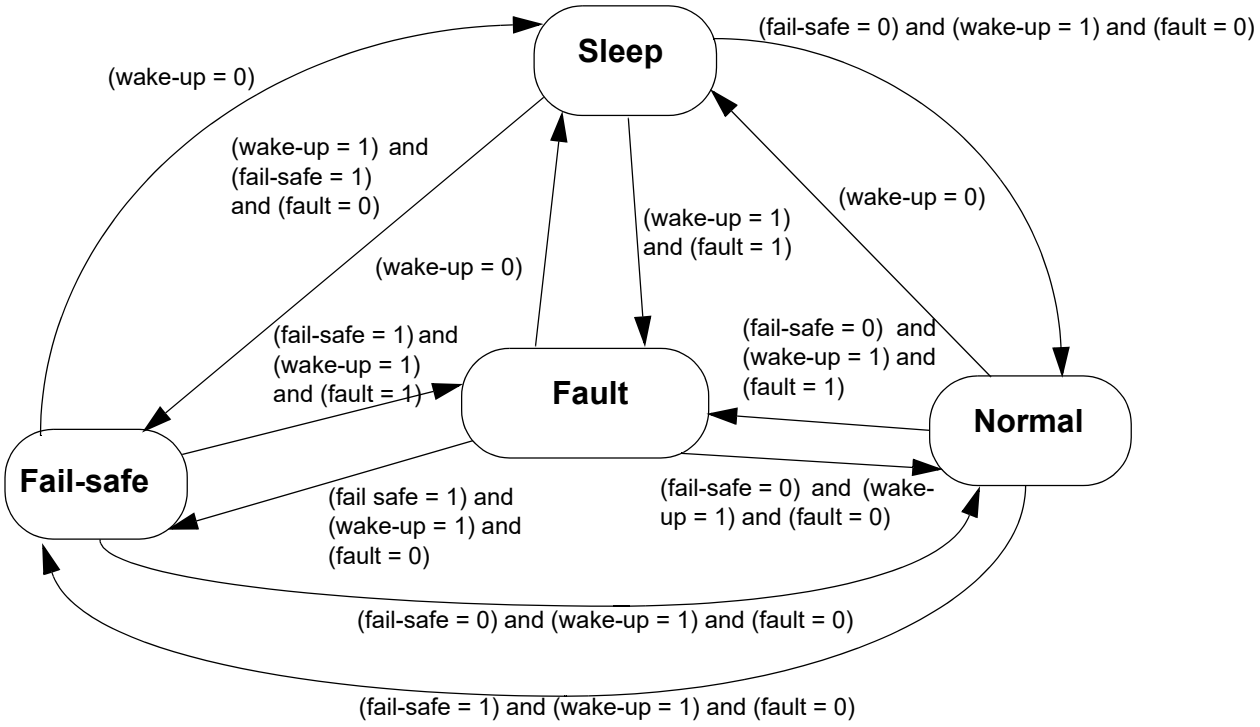



**Figure 12. Device operating modes**

### 6.1.4 Sleep mode

In Sleep mode, the channels and the SPI interface are turned off to minimize current consumption. The device enters Sleep mode (wake-up = 0) when both Direct Input pins IN(x) remain Off longer than $t_{IN}$ sec. (when reset is active; RSTB = 0). This is expressed as follows:

- $V_{PWR}$ (and $V_{DD}$) are within the normal range, and
- wake-up = 0 (wake-up = RSTB or IN_ON[0] or IN_ON[1]) and
- fail-safe = X and
- fault = X

When employed, $V_{DD}$ must be kept in the normal range. Sleep mode is the default mode after the first application of the supply voltage ($V_{PWR}$), prior to any I/O communication (RSTB and the internal states IN_ON[0:1] are still at logic [0]). All SPI register contents remain in their default state during Sleep mode.

### 6.1.5 Fail-safe mode

#### 6.1.5.1 Entering fail-safe mode

Fail-safe mode is entered either upon loss of SPI communication or after loss of optional SPI supply voltage $V_{DD}$ (VDD out of range). The FSOB pin goes low and the channels are only controlled by the direct inputs (IN[0:1]). All protective functions remain fully operational. Previously latched faults are delatched and SPI register contents is reset (except bits POR & PARALLEL). The SPI registers can not be accessed. These conditions are also described by the following expressions:

- $V_{PWR}$ is within the normal voltage range, and
- wake-up = 1, fault = 0, and
- fail-safe = 1 (($V_{DD}$ Failure and $V_{DD}$_FAIL_en=1 before) or (t(SPI)> $t_{WDTO}$ and WD_dis = 0).

The last condition describes the loss of SPI communication which is detailed in the next section.

#### 6.1.5.2 Watchdog on SPI communication and Fail-safe mode

When $V_{DD}$ is present, the SPI watchdog timer is started upon a rising edge on the RSTB pin. Thereafter the device monitors the state of the first bit (WDIN) of all received SPI words. When the state of this bit is not alternated at least once within a data stream of duration $t_{WDTO}$ = 310 ms typ., the device considers that SPI communication has been lost and enters Fail-safe mode. This behavior can be disabled by setting the bit WD_DIS = 1. The value of watchdog timeout is derived from an internal oscillator.

#### 6.1.5.3 Returning from Fail-safe to Normal mode

To exit Fail-safe mode and return to Normal mode again, first a SPI data word with its WDIN bit = 1 (D15) must be received by the device (regardless the register it is contained in and regardless the values of the other bits in this register). Next, a second data word must be received within the timeout period ($t_{WDTO}$ = 310 ms typ.) to be able to change any SPI register contents. Upon entering Normal mode, the FSOB pin returns to logic high and previously set faults and SPI registers are reset, except bits POR, PARALLEL and fault bits of latchable faults that had actually been latched.

### 6.1.6 Fault mode

The device enters Fault mode when any of the following faults occurs in Normal or Fail-safe mode:

- Overtemperature fault, (latchable fault)
- Overcurrent fault, (latchable fault)
- Severe short-circuit fault, (latchable fault)
- Output shorted to $V_{PWR}$ in OFF state (default: disabled)
- Open load fault in OFF state (default: disabled)
- Open load fault in ON state (default: disabled)
- External Clock Failure (default: enabled)
- Overvoltage fault (enabled by default)
- Undervoltage fault, (latchable fault)

The Fault Status pin (FSB) asserts a fault occurrence on any channel in real time (active low). Additionally, the assigned fault bit in the STATR_s or FAULTR_s register is set to one. Conversely to the FSB pin, a fault bit remains set until the corresponding register is read, even if the fault has disappeared. These bits can be read via the SO pin. Fault occurrence results in a turn-off of the incurred channel,

except for the following faults: open load (On and Off state), External Clock Failure and Output(s) shorted to $V_{PWR}$. Under and overvoltage occurrences cause simultaneous turn-off of both channels. Details on the device's behavior after the occurrence of one of the above faults can be found in Protection and diagnostic features.

Fault mode (Operation and operating modes) is entered when:

- $V_{PWR}$ (+$V_{DD}$) were within the normal voltage range, and
- wake-up = 1, and
- fail-safe = X, and
- fault = 1 (see Going from Normal to Fail-safe, Fault or Sleep mode)

#### 6.1.6.1 Resetting fault bits

Registers STATR_s and FAULTR_s contain global and channel-specific fault information. Reading the register the fault bit is contained in clears it, provided failure cause disappearance was detected and the fault wasn't latched.

#### 6.1.6.2 Entering Fault mode from Fail-safe mode

When a Fault occurs in Fail-safe mode, the device is in Fault/Fail-safe mode and behaves according to the description of fault mode. However, SPI registers remain reset and can not be accessed. Only the Direct Inputs control the channels.

#### 6.1.6.3 Returning from Fault mode to Fail-safe mode

When disappearance of the fault previously produced in Fail-safe mode has been detected, the device returns to Fail-safe mode and behaves accordingly. FSB goes high, but the auto-retry counter is not reset. Latched faults are not delatched. SPI registers remain reset.

### 6.1.7 Latchable faults

An auto-retry function (see Auto-retry) controls how the device responds to the so-called latchable faults. Latchable faults are: overcurrent (OC), severe short-circuit (SC), overtemperature (OT), and undervoltage (UV). If a latchable fault occurs, the channel is turned off, the FSB terminal goes low, and the assigned fault bit is set. These bits can not be reset before the next turn-on event is generated by auto-retry. Next, the channel automatically turns on at a programmable interval (provided auto-retry was enabled and the channel wasn't latched).

If the failure disappears prior to the expiration of the available amount of auto-retries, the FSB pin automatically returns to logic [1], but the fault bit remains set. It can then still be reset by reading the SPI register it is contained in.

However, the fault actually gets latched if the failure cause hasn't disappeared at the first turn-on event following expiration of the available amount of auto-retries (see Auto-retry). In that case, the channel gets latched and the FSB terminal remains low. The fault bit can not be reset by reading out the associated SPI register prior to performing a delatch sequence (Fault delatching).

#### 6.1.7.1 Fault delatching

To delatch a latched channel and be able to turn it on again, a delatch sequence must be executed after disappearance of the failure cause. Delatching resets the fault bit of latched faults (see Resetting fault bits). To reset the FSB pin, both channels must be delatched.

Delatching is achieved either by alternating the state of the channels' fault control signal fc[x] (generating a 1_0_1 sequence), or by resetting the auto-retry counter (provided retry is enabled). See Reset of the auto-retry counter. Delatching then actually occurs at the rising edge of the turn-on event.

Signal fc[x] is an internal signal used by the device's internal logic circuitry to control the diagnostic functions. The value of fc[x] depends on the state of the variables IN_ON[x], DIR_dis[x] and ON[x] and is expressed as follows:

fc[x] = ((IN_ON[x] and DIR_dis[x] = 0) or ON[x] = 1)

Alternating the fc[x] signal is achieved differently according to the way the user controls the device.

- In direct-input controlled mode (DIR_dis_s = 0), the IN[x] pin must be set low, remain low for at least $t_{IN}$ seconds, and set high again (be switched On). This might happen automatically when operating at frequencies f<4.0 Hz.
- In SPI-controlled mode, the ON_bit state (D8 of the PWMR_s reg.) must be alternated ('toggled'). No minimum OFF state duration is required in this case.

Performing a delatch sequence anytime during an ongoing auto-retry sequence (before latching) allows turning the channel on unconditionally. When a Power-ON event occurs (see Loss of VPWR, loss of VDD, and power-on reset (POR)), latched channels are also delatched and faults are reset.

When Fail-safe mode is entered (fault =1, fail-safe becomes 1) during operating in Fault mode (fault=1, fail-safe=0), previously latched faults are delatched and SPI register content is reset (except bits POR & PARALLEL). The device is then in a combined Fail-safe/Fault mode. When the device was already in Fail-safe mode (fault = 1, fail-safe =1) and (new) faults occurs, the internal auto-retry counter does not reset and latched channels are not delatched until a delatching sequence has been performed (see Protection and diagnostic features).

## 6.1.8 Programmable PWM module

Each channel has a fully independent PWM module activated by setting PWM_en_s. It modulates an internal or external clock signal. Setting Clock_int_s = 1 (bit D6 of the OCR_s register) activates the internal clock, and setting Clock_int_s = 0 activates the external clock. The duty cycle can be set in a range from 0% to 100% with 8 bit-resolution (Table 7) by setting bits D8…D0 of the PWMR_s register (Table 12). The channel's switching frequency equals the clock frequency divided by 256 in internal clock mode, and by 256 or 512 in external clock mode.

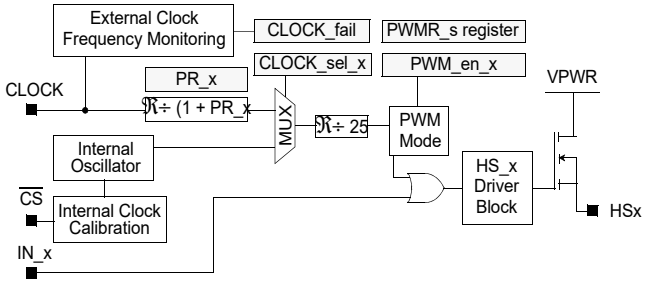



**Figure 13. Internal and external clock operation**

**Table 7. PWM duty cycle value assignment**

| ON-bit | Duty cycle | Channel configuration |
|---|---|---|
| 0 | X | OFF |
| 1 | 00000000 | PWM (duty cycle =1/256) |
| 1 | 00000001 | PWM (duty cycle =2/256) |
| 1 | 00000010 | PWM (duty cycle =3/256) |
| 1 | n | PWM (duty cycle = (n+1)/256) |
| 1 | 11111111 | fully ON |

By delaying the activation of one channel relative to the other (Table 8), switch-on surges can be delayed, which may improve EMC performance. Switch-On delay can be selected among seven different values (default=0) by setting bits D2…D0 of the CONFR_s register (expressed as a number of ext./int. PWM clock periods). To start the PWM function at a known point in time, the PWM_en_s bit (D8 /D7 of the GCR reg.) must be set to 1 after having set the PWMR_s (duty cycle) and CONFR_s (delay) registers. The best way to improve EMC is to use an external clock with a staggered switch on delay.

**Table 8. Switch-on delay in PWM mode**

| Delay bits | Switch-on delay |
|---|---|
| 000 | no delay |
| 001 | 32 PWM clock periods |
| 010 | 64 PWM clock periods |
| 011 | 96 PWM clock periods |
| 100 | 128 PWM clock periods |
| 101 | 160 PWM clock periods |
| 110 | 192 PWM clock periods |
| 111 | 224 PWM clock periods |

### 6.1.8.1 External clock and internal PWM (Clock_int_s = 0)

The channels can be controlled by an external clock signal by setting bit D6 =0 of the OCR_s register (Clock_int_s). Duty cycle values specified in Table 7 apply. When an external clock is used, the value of frequency division (256 when PR[x] = 0) may be doubled by setting the prescaler bit PR[x]) = 1(bit D7 of the OCR_s reg.). This allows driving the channels at different switching frequencies from a single clock signal. Simultaneously setting PWM_en_1=1 and PWM_en_0=1 synchronizes the channels.

The clock frequency on the CLOCK pin is monitored when external clock (CLOCK_int_s = 0) and pulse width modulation (PWM_en_s = 1) are both selected. If a clock failure occurs under these conditions ($f < f_{CLOCK(LOW)}$ or $f > f_{CLOCK(HIGH)}$), the external clock signal is ignored and a fault is detected (FSB =0), CLOCK_fail bit is set (OD2 in the DIAGR register). The state of the ON_s bit in the SPI register then determines the channel's switching state. To return to external clock mode (and reset FSB), the clock-fail bit must be read and the external clock has to be within the authorized range again.

### 6.1.8.2 Internal clock and internal PWM (Clock_int_s bit = 1)

By using a reference time slot (usually available from an external microcontroller), the period of each of the internal PWM clocks can be changed or calibrated (see Programmable PWM module). Calibration of the default period = $1/f_{PWM(0)}$ reduces it maximum variation from about +/-30% to +/-10%. The programming procedure is initialized by sending a dedicated word to the SI-CALR register (see Table 7). Next, the device sets the new value of the switching period in 2 steps. First it measures the time elapsed between the first falling edge on the CSB pin and the next rising edge on the CSB pin ($t_{CSB}$). Then it changes the value of the internal clock period accordingly. The actual value of the channel's switching period is obtained by multiplying the internal clock period by 256.

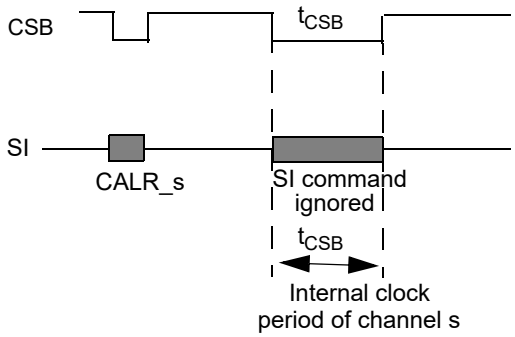



**Figure 14. Internal clock calibration**

When the duration of the negative CSB pulse is outside a predefined time slot (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event is ignored and the internal clock frequency remains unchanged. If the value ($f_{PWM(0)}$) has not been previously calibrated, it remains at its default level.

### 6.1.8.3 Synchronization of both channels

When internal clock signals are used to drive the PWM modules, perfect synchronization over a long time can not be achieved since both clock signals are independent. However, when the channels are driven by an external clock, perfect synchronization can be achieved by simultaneously setting PWM_en_1=1 and PWM_en_0=1. The best way to optimize EMC is to use an external clock with a staggered switch on delay (see Table 8).

## 6.1.9 Parallel operation

The channels can be paralleled to drive higher currents. Setting the PARALLEL bit in the GCR register to logic [1] is mandatory in this case. The improved synchronization of both transistors allows an equal current distribution between both channels. In Parallel mode, both output pins (HS[x]) must be connected (as well as both IN[x] pins in case of external control). CONF0 and CONF1 must be set to equal values.

***1- Device configuration in Parallel mode:***

There are two ways to configure the On/Off control: SPI-configured PWM control and Direct Input Control.

- SPI configured Parallel mode:

The switching configuration is solely defined by the (SI) PWMR_0, CONFR_0, OCR_0, and RETRY_0 registers. As soon as PARALLEL=1, the contents of the corresponding registers in bank 1 are replaced by that of bank 0, except bits D6-D8 of the CONFR_1

register (configuration of the open load/Output short-circuited diagnostics). After setting PARALLEL=1, contents of SO registers in bank 0 are copied to registers of bank 1 only when new information is written in them. Bits OD3, OD4 and OD5 of both FAULTR_s registers (OLON, OLOFF, OS) are always reported independently.

- Direct Input controlled Parallel mode:

The IN0 and IN1 pins must be connected externally.

***2- Diagnostics in Parallel mode:***

The Diagnostics in Parallel mode operate as follows:

- Open load in OFF state and - open load in ON state:

The OL_ON and OL_OFF bits of both FAULTR registers independently report failures of the channels according to the settings of bits D7 and D6 of the CONFR_s register.

- Current sensing: See Table 23 for a description of the various current sensing modes. Only the Current sense ratio of bank 0 (D5 of the OCR_0 register) is considered. The corresponding bit in the OCR_1 register is copied from that of the OCR_0 register.
- output shorted to battery:

The OS-bit (OD3) of each of both FAULT registers independently report this fault, according to the settings of bit D8 of the CONFR_s reg.

***3- Protections in Parallel mode:***

- Overcurrent:

-Only the configuration of overcurrent thresholds and blanking windows of channel 0 are considered.

-If overcurrent (OC) occurs on any channel, both channels are turned-off. Regardless the order of occurrence of OC, both OC-bits (OD0) in the FAULT registers are simultaneously set to logic 1.

- severe short-circuit:

In case of SC detection on any channel, both channels are turned-off and the SC bits (OD1) in both FAULT registers are simultaneously set to logic 1.

- overtemperature:

In case of OT detection on any channel, both channels are turned-off and both OT bits in the FAULT registers (OD2) are simultaneously set to logic 1.

- auto-retry:

Only one 4-bit auto-retry counter specifies the number of successive turn-on events on paralleled channels (RETRYR_0). The counter value in register RETRYR_1 (OD4…OD7) is copied from that in RETRYR_0. To delatch the channels, only channel 0 needs to be delatched.

# 6.2 Protection and diagnostic features

## 6.2.1 Protective functions

### 6.2.1.1 Overtemperature fault (Latchable fault)

The channels have individual overtemperature detection. As soon as a channel's junction temperature rises above $T_{SD}$ (175 °C typ.), it is turned OFF, the overtemperature bit (OT = OD2) is set, and FSB = 0. FSB can only be reset by turning ON the channel when the junction temperature of both channels has dropped below the threshold: $T_J<T_{SD}$. Overtemperature is detected in ON and in OFF state:

- If the channel is ON, the associated output is switched OFF, the OT bit is set, and FSB = 0.
- If the channel is OFF: FSB goes to logic [0] and remain low until the temperature of both channels is below $T_{SD}$ and any of the channels is turned on again.

The auto-retry function (if activated) automatically turns the channel on when the junction temperature has dropped below $T_{SD}$. The OT fault bit can only be reset by reading out the FAULTR register, provided that $T_J<T_{SD}$ and FSB = 1 again.

### 6.2.1.2 Overcurrent fault (Latchable fault)

When overcurrent (OC) is detected, the channel is immediately turned Off (after $t_{FAULT}$ seconds). The OC-bit is set to 1 and FSB becomes low [0]. Overcurrent is detected anytime the load current crosses an overcurrent threshold or exceeds the window width of the selected overcurrent protection profile. This profile is a stair function with windows the height and width of which are preselected through the SPI port. The maximum allowable value of the load current at a particular moment in time is defined by levels $I_{_OCH}$ and $I_{_OCM}$ and windows

$t_{OCM_x}$ and $t_{OCH}$ (programmable by SPI bits). The steady-state overcurrent protection level $I_{_OCL}$ is defined by the settings of the OCL and HOCR bits. Anytime an overcurrent window is active, current sensing is blanked and SYNC becomes 1.

### 6.2.1.3 Overcurrent duration counter

The load current can spend only a defined amount of time in a particular window of the overcurrent profile. If the time in the window exceeds the selected window width ($t_{OCx}$) or the overcurrent threshold is crossed, the channel is turned off (OC fault), followed by auto-retry (if enabled). An internal overcurrent duration counter is employed for this function.

### 6.2.1.4 Overcurrent detection on resistive and inductive loads

According to the load type (resistive or inductive), one of two different overcurrent profiles should be selected. This is done by connecting a resistor with the appropriate value between the CONF[0:1] pins and GND (Table 9).

The overcurrent profile can also be configured through the SPI in the RETRY_s register. If CONF_SPI_s bit is set to 0, the overcurrent profile is selected on the CONF input pin, otherwise it is the opposite. After device reset, the overcurrent profile is defined by the CONF input pin. The SPI-SO CONF bit reporting shall combine external hardware configuration and SPI settings.

**Table 9. Overcurrent profile selection**

| CONF[0:1] resistor/voltage | Type of load |
|---|---|
| 1.0 kΩ < R(CONF[x]) < 10 kΩ or 0 < V(CONF[X) < VIL (0.8 V) | resistive: CONF = 0, Lighting-mode |
| R(CONF[x]) > 50 kΩ or VIH (2.0 V)< V(CONF) < 5.0 V | inductive: CONF = 1, DC motor mode |

When overcurrent windows are active, current sensing is disabled and the SYNCB pin remains high. This is illustrated by Figure 15. After turn on, the output voltage (second waveform) and the output current (first waveform) rise immediately, but the current sense voltage (third waveform) and its synchronization signal SYNC (fourth waveform) only become active at the end of the selected overcurrent window (duration $t_{OCM2_L}$).

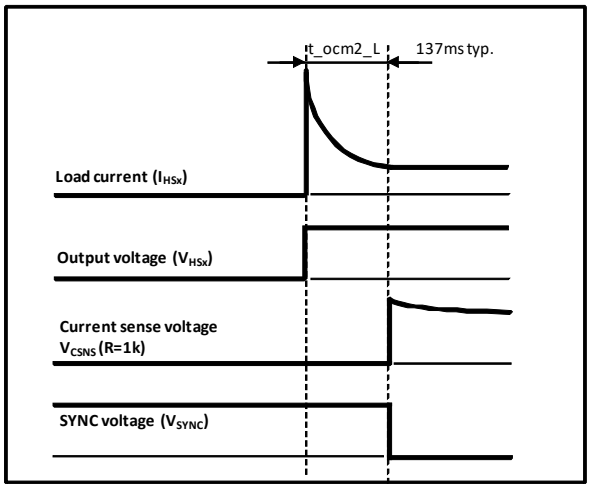



**Figure 15. Current sense blanking during overcurrent window activity**

Activation of the lighting profile is time driven and activation of the DC motor profile is event driven, as explained below.

In lighting mode, the height of the overcurrent profile is defined by three different thresholds ($I_{_OCH}$, $I_{_OCM}$ and $I_{_OCL}$, which stand for the higher, the middle, and the lower overcurrent threshold), as illustrated by Figure 5. This profile has two adjacent windows the width of which is compatible with typical bulb inrush current profiles. The width of the first of these windows is either $t_{OCH1}$ or $t_{OCH2}$. The width of the second window is either $t_{OCM1_L}$ or $t_{OCM2_L}$ (see Table 18). The lighting profile is activated at each turn-on event including auto-retry, except in switch mode. In switch mode, the profile is activated only at the first turn-on event, but is not renewed. During the on-period, the load current is continuously compared to the programmed overcurrent profile. The channel is switched Off when a threshold is crossed or a window width is exceeded.

In DC motor mode, only one overcurrent window exists, defined by only two different thresholds ($I_{_OCH}$ and $I_{_OCL)}$ as illustrated by Figure 6. This window is opened anytime the output current exceeds the selected lower overcurrent threshold ($I_{OCLx}$). In this case, the allowed overcurrent duration is defined by parameters $t_{OCM1_M}$, $t_{OCM2_M}$, $t_{OCH1}$ and $t_{OCH2}$. The selection of the different profiles and values is explained in the section Address A0100— overcurrent protection configuration register (OCR_s).

### 6.2.1.5 Auto-retry after overcurrent shut off

When auto-retry is activated, OC-latching (Overcurrent fault (Latchable fault)) only occurs after expiration of the available amount of auto-retries (described in section Auto-retry).

### 6.2.1.6 Switch mode operation and overcurrent duration

Switch mode is defined as any device operation with a duty cycle lower than 100% at a frequency above $f_{PWM_EXT}$ (min.) or $f_{PWM_INT}$ (min.). The device may operate in Switch mode in internal/external PWM or in Direct input mode. In Switch mode, the accumulated time spent by the load current in a particular window segment during On times of successive switching periods is identified by the aforementioned duration counter, and compared to the active segment width. The associated off-times are excluded by the duration counter. The channel is turned-off when the value of the counter exceeds the window width. In Figure 16, overcurrent detection shutdown is shown in case of switch mode operation with a duty cycle of 50% (solid line) and 100% (fully-on, dashed line). The device is turned off much later in switch mode than in fully-on mode, since the duration counter only counts overcurrent during on-times.

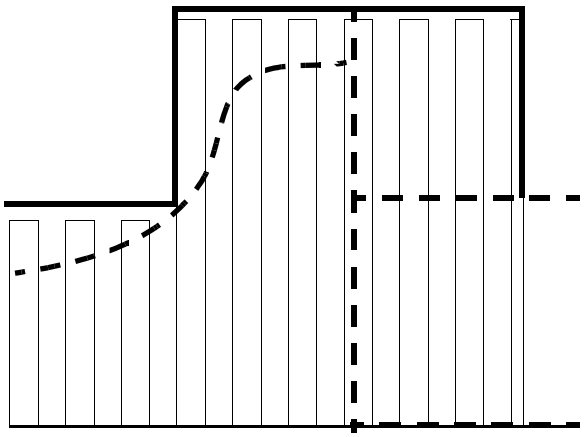


**Figure 16. Overcurrent shutdown in PWM mode (solid line) and fully-on mode (dashed line)**

### 6.2.1.7 Reset of the duration counter

Reset of the duration counter is achieved by performing a delatch sequence (Fault delatching). In lighting mode (CONFs = 0), this counter is also reset automatically at each auto-retry (but not in DC motor mode).

In DC motor mode, the duration counter is reset by a performing a delatch sequence and automatically after a full on-period without overcurrent ([hson[x]=1 for any duration). Reset then actually occurs at the first turn-off instant following that on-period. In switch mode, the duration counter is not reset by normal PWM activity unless delatching is performed.

### 6.2.1.8 Severe short-circuit fault (Latchable fault)

When a severe short-circuit (SC) is detected at turn-ON (wiring length $L_{LOAD} < L_{SHORT}$, see Table 4), the channel is shut off immediately. For wiring lengths above $L_{SHORT}$, the device is protected from short-circuits by the normal overcurrent protection functions (Overtemperature fault (Latchable fault)). When an SC occurs, FSB goes low (logic [0]), and the SC bit is set, eventually followed by an auto-retry. SC is of the latchable fault type (see Protection and diagnostic features and Fault delatching).

### 6.2.1.9 Overvoltage detection (enabled by default)

By default, the supply overvoltage protection ($V_{PWR}$) is enabled. When overvoltage occurs ($V_{PWR} \geq V_{PWR(OV)}$), the device turns OFF both channels simultaneously, the FSB pin is asserted low, and the OV fault bit is set to logic [1]. The channels remain OFF until the supply voltage drops below a threshold voltage $V_{PWR} \leq V_{PWR(OV)} - V_{PWR(OVHYS)}$. The OV bit can then be reset by reading out the STATR register.

The overvoltage protection can be disabled by setting the OV_dis = 1 in the general configuration (GCR) register. In this case, the FSB pin neither asserts a fault occurrence, nor turns off the channels. However, the fault register (OV bit) still reports an overvoltage occurrence (when $V_{PWR} \geq V_{PWR(OV)}$) as a warning. When $V_{PWR} \geq V_{PWR(OV)}$, the value of the on-resistance on both channels ($R_{DS(on)}$) still lays within the ranges specified in Table 4.

### 6.2.1.10 Undervoltage fault (Latchable fault)

The channels are always turned off when the supply voltage ($V_{PWR}$) drops below $V_{PWR(UV)}$. FSB drops to logic [0], and the fault register's (common) UV bit is set to [1]. When the undervoltage condition then disappears, two different cases exist:

- If the channel's internal control signal hson[x] is off, FSB returns to logic [1], but the UV bit remains set until at least one output is turned on (warning).
- If the channel's control signal is on, the channel is turned on if a delatch or POR sequence is performed prior to the turn on request. The UV bit can then only be reset by reading out the STATR register.

Auto-retry (if enabled) starts as soon as the UV condition disappears.

### 6.2.1.11 Extended mode protection

In extended mode (6.0 V < $V_{PWR}$ < 8.0 V or 36 V < $V_{PWR}$ < 58 V), the channels are still fault protected, but compliance with the specified protection levels is not guaranteed. The register settings however (including previously detected faults) remain unaltered, provided $V_{DD}$ is within the authorized range. Below 6.0 V, the channels are only protected from overtemperature, and this fault is only reported in the SPI register the moment $V_{PWR}$ has again risen above $VPWR_{(UV)}$. To allow the outputs to remain ON between 36 V and 58 V, overvoltage detection should be disabled (by setting OV_dis = 1 in the GCR register).

Faults (overtemperature, overcurrent, severe short-circuit, over and undervoltage) are reset if:

- $V_{DD} \leq V_{DD(FAIL)}$ with $V_{PWR}$ in the normal voltage range
- $V_{DD}$ and $V_{PWR}$ are below the $V_{SUPPLY(POR)}$ voltage threshold
- The corresponding SPI register is read after the disappearance of the failure cause (and delatching)

### 6.2.1.12 Drain/source overvoltage protection

The device tries to limit the Drain-to-Source voltage by turning on the channel whenever $V_{DS}$ exceeds $V_{DS(CLAMP)}$. When a fault occurs (SC, OC, OT, UV), the device is rapidly switched Off (in t < $t_{FAULT}$ seconds), regardless the value of the selected slew rate. This may induce voltage surges on $V_{PWR}$ and/or the output pin (HS[x]) when connected to an inductive line/load. Turning on the device also dissipates the energy stored in the inductive supply line. This function monitors overvoltage for $V_{PWR}$ > 30 V. For supply voltages $V_{PWR}$ < 30 V, the device is protected from negative output voltages by automatically turning on the channel. The feature remains functional after device ground loss.

### 6.2.1.13 Supply overvoltage protection

In order to protect the device from excessive voltages on the supply lines, the voltage between the device's supply pins (VPWR and the GND) is monitored. When the $V_{PWR}$-to-GND voltage exceeds the threshold $V_{D_GND(CLAMP)}$, the channel is automatically turned on. The feature is not operational in cases of ground loss.

### 6.2.1.14 Negative output voltage protection

The device tries to limit the undervoltage on the output pins HS[x] when turning off inductive loads. When the output voltage drops below $V_{CL}$, the channel is switched on automatically. This feature is not guaranteed after a device ground loss.

The energy dissipation capabilities of the circuit are defined by the $E_{CL[0:1]}$ parameters. For inductive loads larger than 20 µH, it is recommended to employ a freewheeling diode. The three different overvoltage protection circuits are symbolically represented in Figure 17. The values of the clamping diodes are those specified in Table 4. Coupling factor k represents the current ratio between the current in the supply-voltage measurement-diode (zener) and the current injected into the MOSFET's gate to turn it on.

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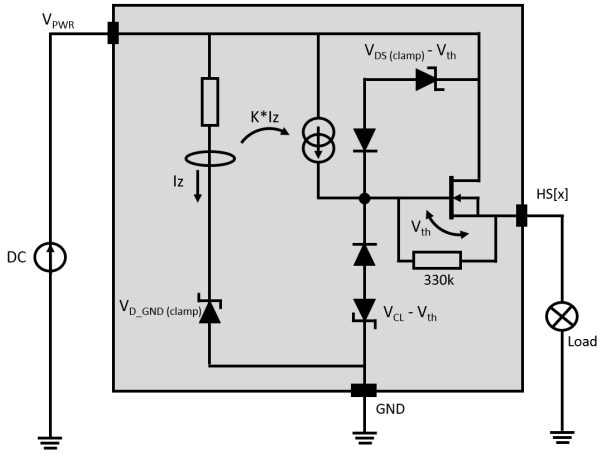



**Figure 17. Supply and output voltage protections**

### 6.2.1.15 Reverse voltage protection on $V_{PWR}$

The device can withstand reverse supply voltages on VPWR down to -32 V. Under these conditions, the outputs are automatically turned On and the channel's On-resistance ($R_{DS(on)}$) is similar to that during positive supply voltages. No additional components are required to protect the $V_{PWR}$ circuit except series resistors (>8.0 k) between the direct inputs IN[0:1] and $V_{PWR}$, in case they are connected to VPWR. The VDD pin needs reverse voltage protection from an externally connected diode (Figure 24).

### 6.2.1.16 Load and system ground loss

In case of load ground loss, the channel's state does not change, but the device detects an open load fault. In case of a system GND loss, the channels are turned off.

### 6.2.1.17 Device ground loss

In the (improbable) case the device loses all of its three ground connections (pins 8, and 28), the channels' state (On/ Off), depends on several factors: the values of the series resistors connected to the device pins, the voltage of the direct input signals, the device's momentary current consumption (influenced by the SPI settings) and the state of other high-side switches on the board when there are pins in common like FSB, FSOB, and SYNC. In the following description, all voltages are referenced to the system (module) GND.

When series resistors are used, the channel state can be controlled by entering Fail-safe mode. The channels are turned off automatically when the voltage applied to the IN[x] input(s) through the series resistor(s) is not higher than $V_{DD}$ and be turned on when the IN[x] input(s) are tied to $V_{PWR}$. Fail-safe is entered under the following conditions:

- all unused pins are tied to the overall system's GND connection by resistors > 8.0 k
- any device pin connected to external system components has a series resistors > 8.0 k (except pins Vpwr, VDD, HS[0], HS[1], and R(CSNS)>2.0 k)
- the FSB, FSOB, and SYNC pins are in the logic high state when they are shared with other devices. This means that none of the other devices is in Fault or Fail-safe mode, nor should current sensing be performed on any one of them when GND is lost

When no series resistors are employed, the channel state after GND loss is determined by the voltage on pins IN[0:1] and the voltage shift of the device GND. Device GND shift is determined by the lowest value of the external voltage applied to either pin of the following list: CLOCK, FSB, IN[0:1], FSOB, SCLK, CS,SI, SO, RSTB, CONF[0:1], SYNC, and CSNS. When the device GND voltage becomes logic low (V(GND)< $V_{IL}$), the SPI port continues to operate and the device operates normally. When the GND voltage becomes logic high (V(GND)> $V_{IH}$), SPI communication is lost and Fail-safe mode is entered. When the voltage applied to the IN[0:1] input is $V_{PWR}$, the channel is turned on when it is $V_{DD}$, the channel is turned off if ($V_{DD}$ - V(GND)) < $V_{IH}$.

## 6.2.2 Supply voltages out of range

### 6.2.2.1 $V_{DD}$ out of range

If the external $V_{DD}$ supply voltage is lost (or falls outside the authorized range: $V_{DD}$<$V_{DD(FAIL)}$), the device enters Fail-safe mode, provided the VDD_FAIL_en bit had been set. Consequently, the contents of all SPI registers are reset. The channels are controlled by the direct inputs IN[0:1] (if $V_{PWR}$ is within the normal range). Since the VPWR pin supplies the circuitry of the SPI, current sense and most of the protective functions (overtemperature, overcurrent, severe short-circuit, short to $V_{PWR}$, and open load detection circuitry), these faults are still detected and reported at the FSB pin. However, without $V_{DD,}$ the SO pin is no longer functional. The SPI registers can no longer be read and detailed fault information is unavailable. Current sensing also becomes unavailable. If $V_{DD_FAIL_EN}$ wasn't set before $V_{DD}$ was lost, the device remains SPI-controlled, even though the SPI registers can't be read. No current flows from the VPWR to the VDD pin.

### 6.2.2.2 $V_{PWR}$ supply voltage out of range

If $V_{PWR}$ is below the undervoltage threshold $V_{PWR(UV)}$, it is still possible to address the device by the SPI port, provided $V_{DD}$ is within the normal range. It does not prevent other devices from operating when a device is part of a daisy-chain. To accomplish this, RSTB must be kept at logic [1]. When the device operates at supply voltages above the maximum supply voltage ($V_{PWR}$=36 V), SPI communication is not affected (see Overvoltage detection (enabled by default)). The internal pull-up and pull-down current sources on the SPI pins are not operational. Executing a Power-on-Reset (POR) sequence is recommended when $V_{PWR}$ re-enters its authorized range. No current flows from the VDD to the VPWR pin.

### 6.2.2.3 Loss of $V_{PWR}$, loss of $V_{DD}$, and power-on reset (POR)

In typical applications (Figure 24 and Figure 25), an external voltage regulator may be used to derive $V_{DD}$ from $V_{PWR}$. In wake mode, a Power-on-Reset (POR) sequence is executed and the POR bit (OD6 of the STATR register) is set when:

- $V_{PWR}$ > $V_{PWR\ (POR)}$, after a period $V_{PWR}$ < $V_{PWR\ (POR)}$ (and $V_{DD}$ < $V_{DD\ (POR)}$ before and after)
- $V_{DD}$ > $V_{DD\ (POR)}$ after a period with $V_{DD}$ < $V_{DD\ (POR)}$ ($V_{PWR}$ < $V_{PWR\ (POR)}$ before and after)

POR is also set at the transition to wake-up (by setting RSTB =1 or IN[x]=1) when $V_{PWR}$ > $V_{PWR\ (POR)}$ (before and after) or $V_{DD}$ >$V_{DD(POR)}$ (before and after). POR is not performed when $V_{PWR}$ > $V_{PWR\ (POR)}$ after a period $V_{PWR}$ < $V_{PWR\ (POR)}$ (and $V_{DD}$ > $V_{DD\ (POR)}$ permanently).

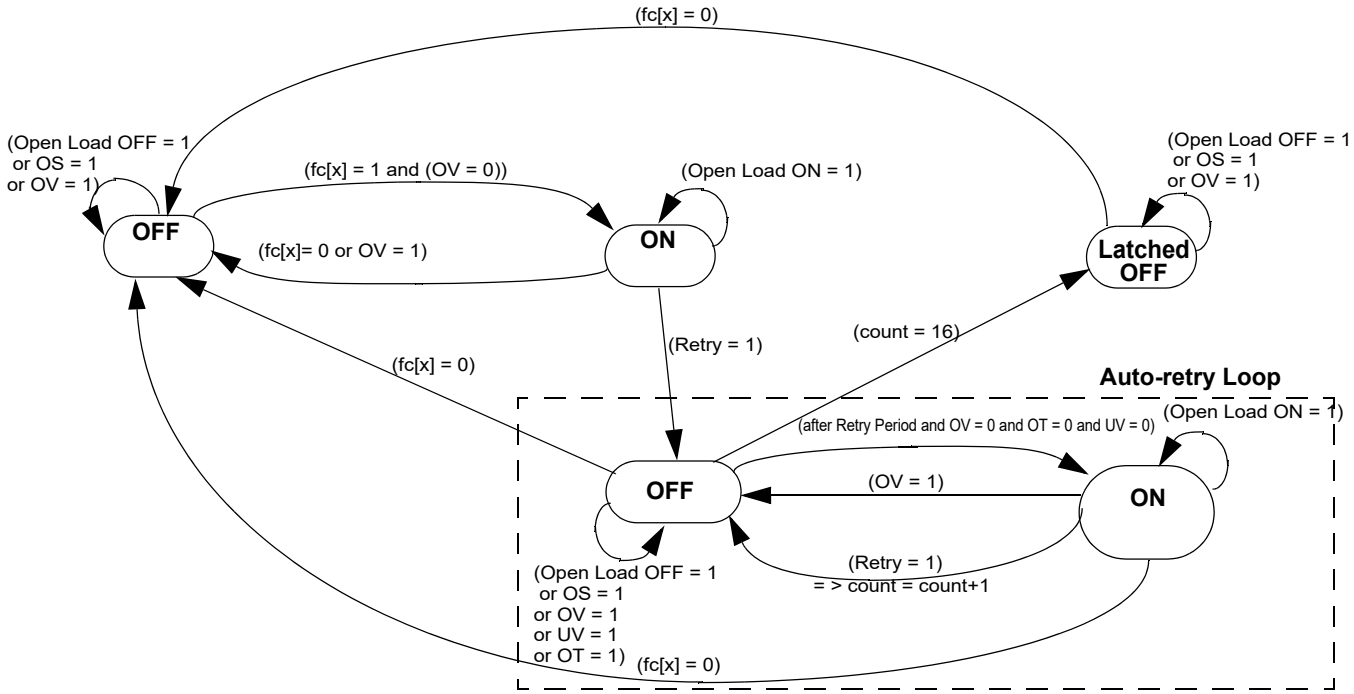



**Figure 18. State machine: fault occurrence and auto-retry**

### 6.2.3 Auto-retry

The auto-retry circuitry automatically tries to turn on the channel on a cyclic basis. Only faults of the latchable type (overcurrent, severe short-circuit, overtemperature (OT), and undervoltage (UV)) may activate auto-retry. For UV and OT faults, auto-retry only starts after disappearance of the failure cause (when auto-retry is enabled). The retry condition is expressed by:

Retry[x] = OC[x] or SC[x] or OT[x] or UV.

If Auto-retry has been enabled, its mode of operation depends on the settings of the auto-retry related bits (bits D0...D3 of the SI-RETRY_s register, see Table 12) and the available amount of auto-retries (bits OD7...OD4 of the SO-RETRY_s reg.). More details can be found in Amount of auto-retries. If Auto-retry is disabled, latchable faults are immediately latched upon their occurrence (see Protection and diagnostic features).

#### 6.2.3.1 Auto-retry configuration

To enable the auto-retry function, bit retry_s (D0 of the SI RETRY_s register) has to be set to the appropriate value. Auto-retry is enabled for retry_s = 0 when the channel is configured for lighting applications (CONF=0). It is enabled for retry_s=1 for DC motor applications (CONF[x] =1).

**Table 10. Auto-retry activation for lamps (CONF=0) and DC motors (CONF=1)**

| CONF[x] | Retry_s bit | auto-retry |
|---|---|---|
| 0 | 0 | enabled |
| 0 | 1 | disabled |
| 1 | 0 | disabled |
| 1 | 1 | enabled |

If auto-retry is enabled, an auto-retry sequence starts when the channel's fault control signal is set to 1 (fc[x] = 1, see Fault delatching) and the retry condition applies (Retry[x]=1, see Auto-retry).

When a failure occurs (fault = 1), the channel automatically switches on again after the auto-retry period. The value of this period ($t_{AUTO}$) is set through the SPI port (bits D2 and D3 of the RETRY_s register, see Table 22). When the failure cause disappears before expiration of the available amount of auto-retries, the device behaves normally (FSB = 1), but the retry counter keeps its current value and the fault bit remains set until it is cleared. This guarantees a maximum device availability without preventing fault detection.

#### 6.2.3.2 Amount of auto-retries

In case the device is configured for an unlimited amount of auto-retries (Retry_unlimited_s = 1), auto-retry continues as long as the device remains powered. The channel never latches off.

In case a limited amount of retries was selected (Retry-unlimited_s = 0), auto-retry continues as long as the value of the 4-bit auto-retry counter does not exceed 15 (bits OD4...OD7 of the RETRY_s register). After 15 retries, the Rfull bit of the STATR (OD4 for channel 0, OD5 for channel 1) register is set to a logic high. The amount of available auto-retries is then reduced to one. If the fault still hasn't disappeared at the next retry, the corresponding channel is switched off definitively and the fault is latched (FSB = 0, see Protection and diagnostic features and Fault delatching).

Any channel can be turned on at any moment during the auto-retry cycle by performing a delatch sequence. However, this does not reset the retry counter. The value of the auto-retry counter can be read back in Normal mode only (SO-RETRYR register bits OD7-OD4).

#### 6.2.3.3 Reset of the auto-retry counter

Any one of the below events reset the retry counter:

- Fail-safe is entered (Fail-safe mode)
- Sleep mode is left (Sleep mode)
- POR occurs (Supply voltages out of range)
- the retry function is set to unlimited (bit Retry-unlimited_s = 1 (D1 = 1))
- the retry function is disabled (retry_s bit= D0 of the RETRY_s register under goes a 1-0 transition for CONF = 1 and a 0-1 transition for CONF = 0).

If the channel is latched the moment the auto-retry counter resets (case 4), the channel is delatched, and turns on after one retry period (if retry was enabled).

#### 6.2.3.4 Auto-retry and overcurrent duration

During the on-period following an auto-retry, the load current profile is compared to the length and height of the selected overcurrent threshold profile, as described in the section on overcurrent protection (See Overcurrent fault (Latchable fault)).

When the lighting profile is activated, the overcurrent duration counter is reset at each auto-retry (to allow sustaining new inrush currents).

For DC motor mode however, it is only reset at the turn-off event of the first PWM period without any overcurrent (see Reset of the duration counter). Figure 18 gives a description of the retry state machine with the various transitions between operating modes.

### 6.2.4 Diagnostic features

Diagnostic functions open load-in-On state (OLON), open load-in-Off-state (OLOFF) and output short-circuited to $V_{PWR}$ (OS) are operational over the frequency and duty cycle ranges specified in Table 5 for PWM mode, but the precise values also depend on the way the device is controlled (direct/internal PWM), on the current sense ratio and on the optional activation of the open load-in-On-state detection. As an example, in direct input (DIR_dis_s = 0), Low-current mode (CSR1), OLON, OLOFF and OS detection are performed for duty cycle values up to: RPWM_400_h = 85% (instead of 90%) when open load in On state detection is enabled (OLON_dis=0).

Occurrence of an OLON, OLOFF or OS fault sets the associated bit in the FAULTR_s register but does not trigger automatic turn-off. Any of these diagnostic functions can be disabled by setting OLON_dis_s=1, OLOFF_dis_s=1, or OS_dis_s=1 (bits D8...D6 of the CONFR reg.). The functions are guaranteed over the specified ranges for output capacitor values up to 22 nF (+/-20%).

#### 6.2.4.1 Output shorted-to-$V_{PWR}$ fault

The device detects short-circuits between the output and VPWR. The detection is performed during the Off-state. The output-shorted-to-VPWR fault-bit (OS_s) is set whenever the output voltage rises above $V_{OSD(THRES)}$. The fault is reported in real time on the FSB pin and saved by the OS_s bit. Occurrence of this fault does not trigger automatic turn-off.

Even if the short-circuit disappears, the OS_s bit is not cleared until the FAULTR register is read. The function may be disabled by setting OS_dis_s=1. The function operates over the duty cycle ranges specified in Diagnostic features. This type of event shall be limited to 1000 min. during the vehicle lifetime. In case of permanent output shorted to the battery condition, it is needed to turn-on the corresponding channel.

#### 6.2.4.2 Open load detection in Off state

Open load-in-OFF-state detection (OL_OFF) is performed continuously during each OFF-state (both for CSR0 and CSR1). This function is implemented by injecting a small current into the load ($I_{OLD(OFF)}$). When the load is disconnected, the output voltage rises above $V_{OLD(THRES)}$. OL_OFF is then detected and the OL_OFF bit in the FAULTR register is set. If disappearance of the open load fault is detected, the FSB output pin returns to a high immediately, but the OL_OFF bit in the fault register remains set until it is cleared by a read out of the FAULTR register. The function may be disabled by setting OLOFF_dis_s=1. The function operates over the duty cycle ranges specified in Diagnostic features.

#### 6.2.4.3 Open load detection in On state (OL_ON)

Open load in ON state detection (OLON) is performed continuously during the On state for CSR0 over the ranges specified in section Diagnostic features. An open load in On state fault is detected when the load current is lower than the open load current threshold $I_{OLD(ON)}$. This happens at $I_{OLD(ON)}$ = 150 mA (typ.) for high-current sense mode (CSR0), and at 7.0 mA (typ.) for low-current mode. FSB is asserted low and the OLON bit in the fault register is set to 1 but the channel remains On. FSB goes high as soon as disappearance of the failure cause is detected, but the OL_ON bit remains set.

In High-current mode (CSR0), open load in On state detection is done continuously during the On state and the OLON-bit remains set even if the fault disappears.

In high-current mode, the OLON-bit is cleared when the FAULTR register is read during the Off state, even if the fault hasn't disappeared. The OLON-bit is also cleared when the FAULTR register is read during the ON state, provided the failure cause (load disconnected) has disappeared.

In low-current mode (CSR1), OL_ON is done periodically instead of continuously and only operates when fast slew rate is selected. When the internal PWM module is used with an internal or external clock (case 1), the period is 150 ms (typ.). When the direct inputs are used (case 2), the period is that of the input signal. The detection instants in both cases are given by the following:

1. In **internal PWM (int./ext. clock)**, low-current mode (CSR1), open load in ON state detection is not performed each switching period, but at a fixed frequency of about 7.0 Hz (each $t_{OLLED}$ =150 ms typ.). The function is available for a duty cycle of 100%.

OLON detection is also performed at 7.0 Hz, at the first turn-off event occurring 150 ms after the previous OL_ON detection event (before OS and OL_OFF).

2. In **direct input**, low-current mode (CSR1), OL_ON is performed each switching period (at the turn-off instant) but the duty cycle is restricted to the values. Consequently, when the signal on the IN[x] pin has a duty cycle of 100%, OL_ON is not performed. To solve this problem, either the internal PWM function must be activated with a duty cycle of 100%, or the channel's direct input must be disabled by setting Dir_dis_s=1 (bit D5 of the CONFR-s register). The OLON-bit is only reset when the FAULTR register is read after occurrence of an OL_ON detection event without fault presence.

#### 6.2.4.4 Open load detection in discontinuous conduction mode

If small inductive loads (solenoids / DC motors) are driven at low frequencies, discontinuous conduction mode may occur. Undesired open load in On state errors may then be detected, as the inductor current needs some time to rise above the open load detection threshold after turn-on. This problem can be solved by increasing the switching frequency or by disabling the function and activating open load in Off state detection instead.

When small DC motors are driven in discontinuous conduction mode, undesired open load in Off state detection may also occur when the load current reaches 0.0 A during the Off state. This problem can be solved by increasing the switching frequency or by enabling open load in Off state detection only during a limited time, preferably directly after turn-off (see Diagnostic features). The signal on the SYNC pin can be used to identify the turn-off instant.

### 6.2.5 Current and temperature sensing

The scaled values of either of the output currents or the temperature of the device's GND pins (8 and 25) can be made available at the CSNS pin. To monitor the current of a particular channel or the general device temperature, the CSNS0_en and CSNS1_en bits (see Table 23) in the General Configuration Register (GCR) must be set to the appropriate values. When overcurrent windows are active, current sensing is disabled and the SYNCB pin remains high.

#### 6.2.5.1 Instantaneous and sampled current sensing

The device offers two possibilities for load current sensing: instantaneous (synchronous) sensing mode and Track & Hold mode (see Figure 9). In synchronous mode, the load current is mirrored through the current sense pin (Output current monitoring (CSNS)) and is therefore synchronous with it. After turn-off, the current sense pin does not output the channel current. In Track & Hold mode however, the current sense pin continues to mirror the load current as it was just before turn-off. Synchronous mode is activated by setting the T_H_en bit to 0, and Track & Hold mode by setting the T_H_en bit to 1.

#### 6.2.5.2 Current sense ratio selection

The load current is mirrored through the CSNS pin with a sense ratio (Figure 19) selected by the CSNS_ratio bit in the OCR register. To achieve optimal accuracy at low current levels, the lower current sensing ratio, called CSR1, must be selected. In that case, the overcurrent threshold levels are decreased. The best accuracy that can be obtained for either ratio is shown in Figure 21. The amount of current the CSNS pin can sink is limited to $I_{CSNS,MAX.}$.The CSNS pin must be connected to a pull-down resistor (470 Ω < R(CSNS) <10 kΩ, 1.0 kΩ typical), in order to generate a voltage output. A small low-pass filter can be used for filtering out switching transients (Figure 24). Current sensing operates for load currents up to the lower overcurrent threshold (OCLx A).

#### 6.2.5.3 Synchronous current sensing mode

For activation of synchronous mode, T_H_en must be set to 0 (default). After turn-on, the CSNS output current accurately reflects the value of the channel's load current after the required settling time. From this moment on (CSNS valid), the SYNC pin goes low and remains low until a switch off signal (internal/external) is received. This allows synchronization of the device's current sensing feature with an external process running on a separate device (see Current sense synchronization (SYNC)). After turn-off, the load current does not flow through the switch, and the load current cannot be monitored.

#### 6.2.5.4 Track & Hold current sensing mode

In Track & Hold mode (T&H) (T_H_en = 1), conversely from synchronous mode, the CSNS output current is available even after having switched off the load. This feature is useful when the device operates autonomously (internal clock/PWM), since it allows current monitoring without any synchronization of the device. An external sample and hold (S/H) capacitor is not required. After turn on, the CSNS output current reflects the channel's load current with the specified accuracy after occurrence of the negative edge on the SYNC pin, as

in synchronous mode (see Current sense synchronization (SYNC)). However, at the switch-off instant, the last observed CSNS current is sampled and its value saved, thanks to an internal S/H capacitor. The SYNC pin goes high (SYNC = 1). If the channel on which Track & Hold current sensing is performed is changed to another, the internal S/H hold capacitor is first emptied and then charged again to allow current monitoring of the other channel. Consequently, T&H current monitoring of a channel is lost when this channel is in the Off state at the moment the current is monitored on the other channel. Track & Hold mode should not be used for frequencies below 60 Hz. When Track & Hold is used to sense the temperature and then to sense a current, the Track & Hold mode has to be reset by a turn off, then turn on before sensing a new current.

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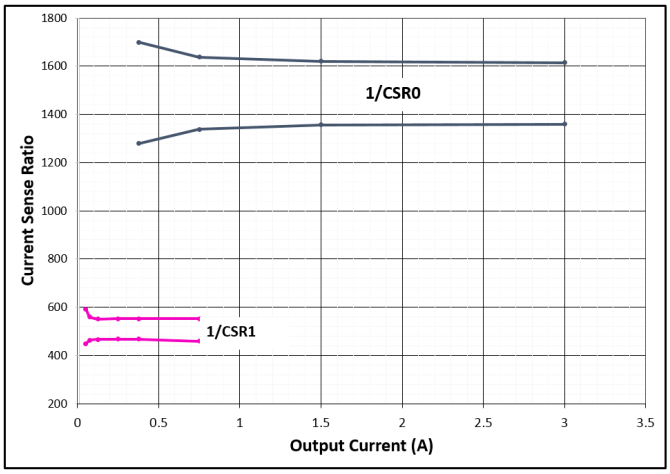



**Figure 19. Current sensing ratio versus output current**

Figure 20 shows how the limits are constructed in Figure 19. The limits are Six-Sigma with regards to the population. CSR1 limits are constructed like CSRO.

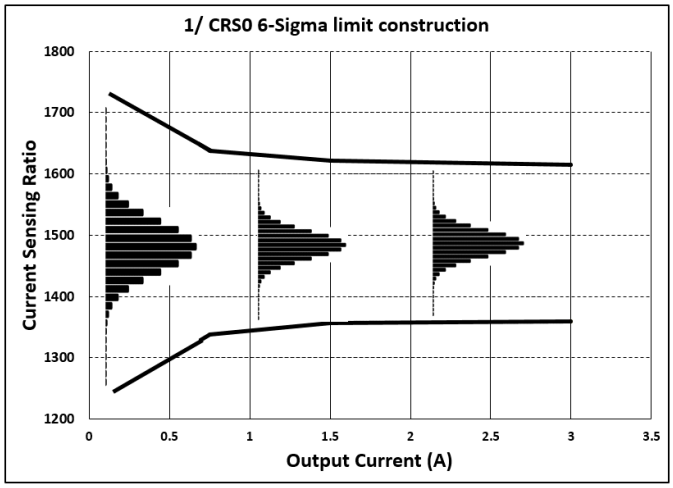



**Figure 20. Current sensing ratio versus output current**

## 6.2.5.5 Current sense errors

Current sense accuracy is adversely affected by errors of the internal circuitry's current sense ratio and offset. The value of the current sensing output current can be expressed with sufficient accuracy by the following equation:

$I_{CSNS}$ = (I(HS[x])+ $I_{_LOAD_ERR_SYS}$ + $I_{_LOAD_Err_RAND}$)*$C_{SRx(1)}$ with $C_{SR0}$ = (1/1500+$\varepsilon_{GAIN0}$) and $C_{SR1}$ = (1/500+$\varepsilon_{GAIN1}$).

The device's offset error has a "systematic" and a "random" component ($I_{_LOAD_ERR_SYS}$, $I_{_LOAD_ERR_RAND}$). At low current levels, the random offset error may become dominant. The systematic offset error is caused by predictable variations with supply voltage and temperature, and has a small but positive value with small spread. The random offset error is a randomly distributed parameter with an average value of zero, but with high spread. The random offset error is subject to part-to-part variations and also depends on the values of supply voltage and device temperature. The device has a special feature called offset compensation, allowing an almost complete

compensation of the random offset error (see $E_{SR0_ERR}$). This offset compensation technique greatly minimizes this error. Computing the compensated current sensing value is illustrated in the next sections.

### 6.2.5.6 Activation and use of offset compensation

According to the settings of the OFP_s bit (in the RETRYR_s register), opposite values of the random offset error are generated. To compensate the random offset error, two separate measurements with opposite values of the random offset error are required. The measured values must be saved by an external µ-processor. Compensation of the random offset error is achieved by computing the average of both. When a dedicated bit called Offset Positive (OFP = bit D8 of the RETRYR_s register) is set to 1, the current sunk through the CSNS pin ($I_{CSNS}$) can be described by:

$$I_{CSNS1}=CSR_x *(I_{LOAD}+ I_{_LOAD_ERR_SYS}+ I_{_LOAD_ERR_RAND}) \quad (2)$$

When bit OFP is set to 0, $I_{CSNS}$ can be described by:

$$I_{CSNS2} = CSR_x *(I_{LOAD}+ I_{_LOAD_ERR_SYS} - I_{_LOAD_ERR_RAND}) \quad (3)$$

The random offset term $I_{_LOAD_ERR_RAND}$ can be computed from equations (2) and (3) as follows:

$$I_{_LOAD_ERR_RAND} = (I_{CSNS1} - I_{CSNS2}) / (2*CSR_x) \quad (4)$$

The compensated current sense value $I_{CSNS,COMP}$ can be obtained by computing the average value of measurements $I_{CSNS1}$ and $I_{CSNS2}$ as follows:

$$I_{CSNS,COMP} = (I_{CSNS1} + I_{CSNS2}) / 2 \quad (5)$$

When equations 2 and 3 are substituted in equation 5, the random offset error cancels out, as shows eq. 6:

$$I_{CSNS,COMP} = (I_{_LOAD_ERR_SYS} + I_{LOAD}) * CSR_x \quad (6)$$

The systematic offset error $I_{_LOAD_ERR_SYS}$ is referenced at the operating point 28 V and 25 °C. It can eventually be fine tuned by performing a calibration. Gain errors at 25 °C (=current sense ratio errors, represented by $\varepsilon_{GAIN0}$ and $\varepsilon_{Gain1}$) can also be reduced by performing a calibration at a point in the range of interest. If calibration can not be done, it is recommended to use the typical value of $I_{_LOAD_ERR_SYS}$ (see $E_{SR0_ERR}$).

### 6.2.5.7 Current sense error model

The figures of uncompensated and compensated current sense accuracy mentioned in Table 4 have been obtained applying the error model of eq. 7 to the data:

$$I_{CSNS_MODEL} = (I(HS[x])+ I_{_LOAD_ERR_SYS}) * C_{SRx} \quad (7)$$

$$E_{SRx_ERR} = (I_{CSNS1} - I_{CSNS_MODEL})/I_{CSNS_MODEL} \quad (8)$$

$$E_{SRx_ERR(COMP)}= (I_{CSNS,COMP} - I_{CSNS_MODEL})/I_{CSNS_MODEL} \quad (9)$$

The computation has been applied to each of the specified measurement points. Model parameters $I_{_LOAD_ERR_SYS}$ and $C_{SRx}$ have the nominal values, specified in $E_{SR0_ERR}$.

The load current can be computed from this model as:

$$I(HS[x]) = I_{CSNS} / CSR_x - I_{_LOAD_ERR_SYS} \quad (10)$$

$$I(HS[x]) = I_{CSNS,COMP} / CSR_x - I_{_LOAD_ERR_SYS} \quad (11)$$

Using expression (11) generally gives more accurate values than expression (10), since in expression (11), random offset errors have been compensated.

### 6.2.5.8 Offset compensation in Track & Hold mode

In Track & Hold mode, the last observed sense current ($I_{CSNS}$) is sampled at the switch off instant. This takes into account the currently active settings of the OFP_s offset compensation bit. Changing the value of the OFP bit during the switch's off time produces an identical value of the current sense output. Consequently, to implement the before mentioned offset compensation technique, the channel must have been turned on at least once prior to sensing the output current with an opposite value of the OFP bit.

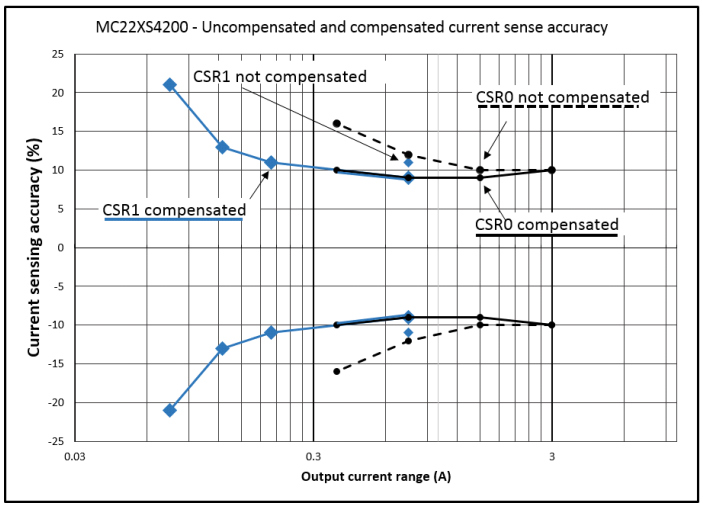
### 6.2.5.9 System requirements for current monitoring

Current monitoring is usually implemented by reading the (RC-filtered) voltage across the pull-down resistor connected between the CSNS pin and GND (Figure 24). Therefore, measurements (1) and (2) must be spaced sufficiently wide apart (e.g. 5 time constants) to get stabilized values, but close enough to be sure that the offset value wasn't changed. The A/D converter of the external micro controller that is used to read the current sense voltage V(csns) must have sufficient resolution to avoid introducing additional errors.

### 6.2.5.10 Accuracy with and without offset compensation

The sensing accuracy for CSR0 and CSR1, obtained before and after offset compensation, is shown in Figure 21 (solid lines = full scale accuracy with offset compensation and dotted lines without offset compensation).

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Notes

43. Accuracy ranges are six-sigma constructed.

**Figure 21. Current sense accuracy versus output current**

In Track & Hold mode, the accuracy of the current sense function is lowered according to the values shown in Figure 22 (error percentage as a function of the switch-off time is displayed, for CSR0 and CSR1). Track & Hold mode should not be used below f = 60 Hz.

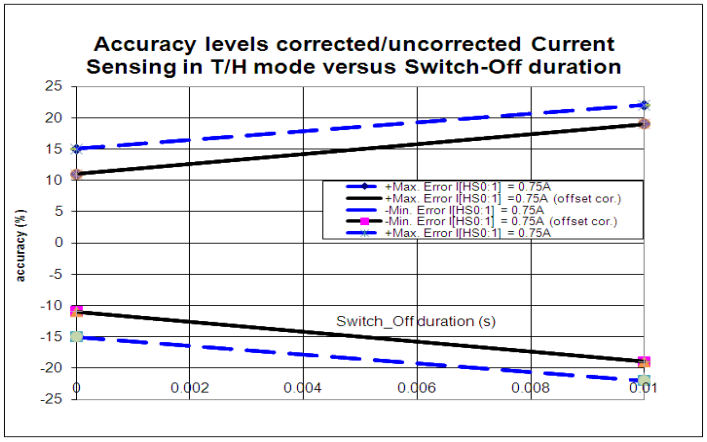



**Figure 22. Track & Hold current sense accuracy**

### 6.2.5.11 Temperature prewarning detection

In Normal mode, the temperature prewarning (OTW) bit is set (bit OD8 of the FAULTR register) when the observed temperature of the GND pin is higher than $T_{OTWAR}$ (pin #14, see Figure 3). The feature is useful when the temperature of the direct surroundings of the device must be monitored. However, the channel isn't switched off. To be able to reset the OTW-bit, the FAULTR register must be read after the moment that temperature T °C < $T_{OTWAR}$.

### 6.2.5.12 Switching state monitoring

The switching state (On/Off) of the channels is reported in real time by bits OUT[x] in the STATR register (bit OD0/OD1). The Out[x] bit is asserted logic high when the channel is on (output voltage V(HS[x]) higher than $V_{PWR}$ /2). When supply voltage $V_{PWR}$ drops below 13 V, the reported channel state may not correspond to the state of the channel's control signal hson[x] in case of an open load fault (see Factors determining the channel's switching state).

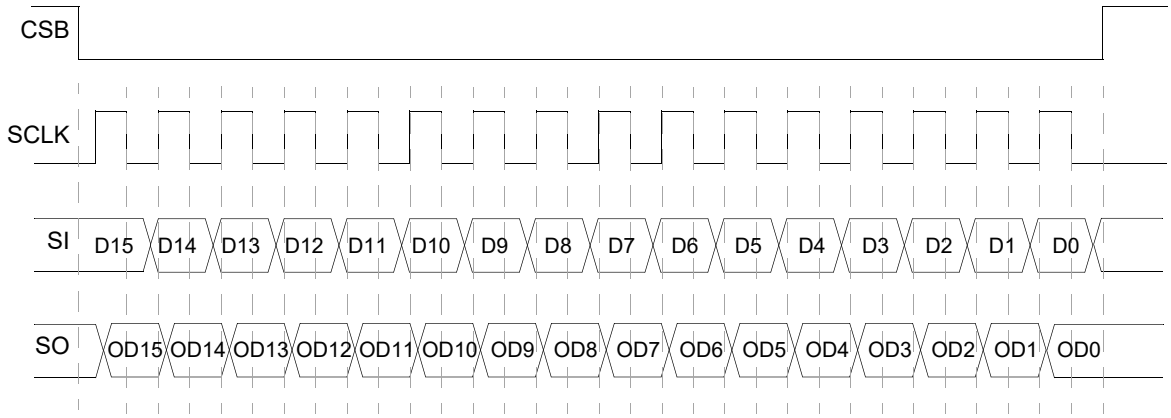
## 6.2.6 EMC performances

Specified EMC performance is board and module dependent and applies to a typical application (Figure 24). The device withstands transients per ISO 7637-2 /24 V. The device meets CISPR-25 Class5 from 1.0 MHz to 1.0 GHz peak. See application AN5000 for EMC result details.

# 6.3 Logic commands and SPI registers

## 6.3.1 SPI protocol description

The SPI interface offers full duplex, synchronous data transfer over four I/O lines: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select (CSB).The SI/SO pins of the device follow a first-in first-out (D15 to D0) protocol. Transfer of input and output words starts with the most significant bit (MSB). All inputs are compatible with 5.0 or 3.3 V CMOS logic levels. Parity check is performed after transfer of each 16-bit SPI data word.The SPI interface can be driven without series resistors provided that voltage ratings on the VDD and SPI pins (Table 3) aren't exceeded. Unused SPI pins must be tied to GND, eventually by resistors (see Device ground loss).




Notes 1. $\overline{RSTB}$ must be in a logic [1] state during data transfer.
2. Data enter the SI pin starting with D15 (MSB) and ending with bit D0.
3. Data are available on the SO pin starting with bit 0D15 (MSB) and ending with bit 0(OD0).

**Figure 23. 16-bit SPI interface timing diagram**

## 6.3.2 Serial input communication protocol

SPI communication requires that RSTB = high. SPI communication is accomplished with 16-bit messages. A valid message must start with the MSB (D15) and end with the LSB (D0) (Table 11). Incoming messages are interpreted according to Table 12. The MSB, D15, is the watchdog bit (WDIN). Bit D14, Parity check (P), must be set such that the total number of 1-bits in the SPI word is even (P=0 for an even number of 1-bits and P=1 for an odd number). Bank selection is done by setting bit D13. Bits D12:D10 are used for register addressing. The remaining ten bits, D9:D0, are used to configure the device and activate diagnostic and protective functions. Multiple messages can be transmitted for applications with daisy chaining (or to validate already transmitted data) by keeping the CSB pin at logic

0. Messages with a length different from a multiple of 16 or with a parity error is ignored. The device has thirteen input registers for device configuration and thirteen output registers containing the fault/device status and settings. Table 12 gives the SI register function assignment. Bit names with extension "_s" refer to functions that have been implemented independently for each of both channels.

## 6.3.3 Serial port operation

When Chip Select occurs (1-to-0 transition on the CSB pin), the output register data is clocked out of the SO pin (MSB-first) at the serial clock frequency (SLCK). Bits at the SI pin are clocked in at the same time. The first sixteen SO register bits are those addressed by the previous SI word (bit D13, D2…D0 of the STATR_s input register). At the end of the chip select event (0-to-1 transition), the SI register contents are latched. The second SPI word clocked out of the Serial Output (SO) after the first CSB event represents the initial SO register contents. This allows daisy chaining and data integrity verification.

The message length is validated at the end of the CSB event (0-to-1 transition). If it is valid (multiples of 16, no parity error), the data is latched into the selected register. After latch-in, the SO pin is tri-stated and the status register is updated with the latest fault status information.

### 6.3.3.1 Daisy chain operation

Daisy-chaining propagates commands through devices connected in series. The commands enter the device at the SI pin and leave it by the SO pin, delayed by one command cycle of 16 bits. To address a particular device in a daisy chain, the CSB pin of all the devices in that chain has to be kept low until the SPI message has arrived at its destination. Once the command has been clocked in by the addressed device, it can be executed by setting CSB=1.

**Table 11. SI message bit assignment**

| Bit n° | SI reg. bit | Bit functional description |
|---|---|---|
| MSB<br>.<br>.<br>.<br>LSB | D15 | Watchdog in (WDIN): Its state must be alternated at least once within the timeout period |
| | D14 | Parity (P) check. P-bit must be set to 0 for an even number of 1-bits and to 1 for an odd number. |
| | D13 | Selection between SI registers from bank 0 (0= channel 0) and bank 1 (Table 14) |
| | D12:D10 | Register address bits |
| | D9:D0 | Used to configure the device and the protective functions and to address the SO registers |

**Table 12. Serial input register addresses and function assignment**

| SI register | SI data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D 15 | D 14 | D 13 | D 12 | D 11 | D 10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| STATR_s | WDIN | P | $A_0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOA2 | SOA1 | SOA0 |
| PWMR_s | WDIN | P | $A_0$ | 0 | 0 | 1 | 0 | ON_s | PWM7_s | PWM6_s | PWM5_s | PWM4_s | PWM3_s | PWM2_s | PWM1_s | PWM0_s |
| CONFR_s | WDIN | P | $A_0$ | 0 | 1 | 0 | 0 | OS_dis_s | OLON_dis_s | OLOFF_dis_s | DIR_dis_s | SR1_s | SR0_s | DELAY2_s | DELAY1_s | DELAY0_s |
| OCR_s | WDIN | P | $A_0$ | 1 | 0 | 0 | 0 | HOCR_s | PR_s | Clock_int_s | CSNS_ratio_s | $t_{OCH_s}$ | tOCM_s | OCH_s | OCM_s | OCL_s |
| RETRY_s | WDIN | P | $A_0$ | 1 | 0 | 1 | 0 | OFP_s | 0 | 0 | 0 | CONF_SPI_s | Auto_period1_s | Auto_period0_s | Retry_unlimited_s | retry_s |
| GCR | WDIN | P | 0 | 1 | 1 | 0 | 0 | PWM_en_1 | PWM_en_0 | PARALLEL | T_H_en | WD_dis | $V_{DD_FAIL_en}$ | CSNS1_en | CSNS0_en | OV_dis |
| CALR_s | WDIN | P | $A_0$ | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| contents after reset* | 0 | X | 0 | X | X | X | 0 | 0 | 0 | 0** | 0 | 0 | 0 | 0 | 0 | 0 |

* = RSTB = 0 or $V_{DD}$(FAIL) after $V_{DD}$ = 5.0 V or POR
** = except bit D6 (PARALLEL) of the GCR register that is saved when $V_{DD}$(FAIL) occurs, provided $V_{DD}$ = 5.0 V and $V_{DD_FAIL_EN}$ = 1 before
X = register address, P = parity bit

**Table 13. Serial output register bit assignment**

| | bits D13, D2, D1, D0 of the previous STATR | | | | SO returned data | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SOA3 | SOA2 | SOA1 | SOA0 | OD15 | OD14 | OD13 | OD12 | OD11 | OD10 | OD9 | OD8 | OD7 | OD6 | OD5 | OD4 | OD3 | OD2 | OD1 | OD0 |
| STATR | 0 | 0 | 0 | 0 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | OV | UV | POR | R_FULL1 | R_FULL0 | FAULT1 | FAULT0 | OUT1 | OUT0 |
| FAULTR_s | $A_0$ | 0 | 0 | 1 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | OTW | 0 | 0 | OLON_s | OLOFF_s | OS_s | OT_s | SC_s | OC_s |
| PWMR_s | $A_0$ | 0 | 1 | 0 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | ON_s | PWM7_s | PWM6_s | PWM5_s | PWM4_s | PWM3_s | PWM2_s | PWM1_s | PWM0_s |
| CONFR_s | $A_0$ | 0 | 1 | 1 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | OS_dis_s | OLON_dis_s | OLOFF_dis_s | DIR_dis_s | SR1_s | SR0_s | DELAY2_s | DELAY1_s | DELAY0_s |
| OCR_s | $A_0$ | 1 | 0 | 0 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | HOCR_s | PR_s | Clock_int_s | CSNS_ratio_s | tOCH_s | tOCM_s | OCH_s | OCM_s | OCL_s |
| RETRYR_s | $A_0$ | 1 | 0 | 1 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | OFP | R3 | R2 | R1 | R0 | Auto_period1_s | Auto_period0_s | Retry_unlimited_s | retry_s |
| GCR | 0 | 1 | 1 | 0 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | PWM_en_1 | PWM_en_0 | PARALLEL | T_H_en | WD_dis | VDD_Fail_en | CSNS1_en | CSNS0_en | OV_dis |
| DIAGR | 0 | 1 | 1 | 1 | WDIN | PF | SOA3 | SOA2 | SOA1 | SOA0 | NM | CONF1 | CONF0 | ID1 | ID0 | IN1 | IN0 | CLOCK_fail | CAL_fail1 | CAL_fail0 |
| contents after reset or failure* | N/A | N/A | N/A | N/A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0** | 0*** | 0 | 0 | 0 | 0 | 0 |

* = RSTB = 0 or $V_{DD}$(FAIL) after $V_{DD}$ = 5.0 V, or POR
** = except bit D6 (PARALLEL) of the GCR register that is saved when $V_{DD}$(FAIL) occurs provided $V_{DD}$ = 5.0 V and VDD_Fail_en = 1 before
*** = except bit D7 (POR) of the STATR register that is saved when $V_{DD}$(FAIL) occurs after $V_{DD}$ = 5.0 V and VDD_Fail_en = 1 (fail-safe mode)
x = register address, PF = parity Fault

## 6.3.4 SI register addressing

The address in the title of the following sections ($A_0$xxx) refer to bits D[13:10] of the SPI word required to address the associated SI register. Bit $A_0$ = D13 selects between registers of bank 0 and bank 1 (Table 14). The function assignment of register bits D[8:0] is described in the associated section. The "_s" behind a register name indicates that the variable applies to the register contents of both banks.

**Table 14. Value of bit $A_0$ required for addressing register banks 0 or 1**

| Value $A_0$ (D13) | Bank |
|---|---|
| 0 | 0 = channel 0 (default) |
| 1 | 1 = channel 1 |

## 6.3.5 Address $A_0$000—status register (STATR_s)

To read back the contents of any of the 13 SO registers, bits D[13:10] of the channel's SI STATR register must be set to $A_0$000 and bits D[2:0] in the same SPI word to the address of the desired SO register. The SO registers thus addressed are: STATR, FAULTR_s, PWMR_s, CONFR_s, OCR_s, RETRY_s, GCR, and DIAGR (Table 13).

## 6.3.6 Address $A_0$001— PWM control register (PWMR_s)

The PWMR_s register contents determines the value of the PWM duty cycle at the output (Table 12), both for internal and external clock signals.

Bit D8 must be set to 1 to activate this function. The desired value of duty cycle is obtained by setting Bits D7:D0 to one of the 256 levels as shown in Table 7. To start the PWM function at a known point in time, the PWM_en_s bit (both in the GCR register) must be set to 1.

## 6.3.7 Address $A_0$010—channel configuration register (CONFR_s)

The CONFR_s is used to select the appropriate value of slew rate and turn-ON delay. The settings of Bits D[8:6] determine the activation of open load and short-circuit (to $V_{PWR}$) detection. Bit D13 ( = $A_0$) of the incoming SPI word determines which of both CONFR registers is addressed (Table 14).

Setting bit D8 (OS_dis_s) to logic [1] disables detection of short-circuits between the channel's output pin and the VPWR pin. The default value [0] enables the feature.

Setting bit D7 (OLON_dis_s) to logic [1] disables detection of open load in the On state for the selected channel. The default value [0] enables this feature (Table 15).

Setting bit D6 (OLOFF_dis_s) to logic [1] disables detection of open load in the OFF state. The default value [0] enables the feature, see Table 15.

**Table 15. Selection of open load detection features**

| OLON_dis_s (D7: On state) | OLOFF_dis_s (D6: Off state) | Selected open load detection function |
|---|---|---|
| 0 | 0 | both enabled (default) |
| 0 | 1 | Off state detection disabled |
| 1 | 0 | On state detection disabled |
| 1 | 1 | Both disabled |

Setting bit D5 (DIR_DIS_s) to logic [0] enables direct control of the selected channel. Setting bit D5 to logic [1] disables direct control. In that case, the channel state is determined by the settings of the internal PWM functions.

D4:D3 bits (SR1_s and SR0_s) control the slew rate at turn on and turn off (Table 16). The default value ([00]) corresponds to the medium slew rate. Rising and falling edge slew rates are identical.

**Table 16. Slew rate selection**

| SR1_s (D4) | SR0_s (D3) | Slew rate |
|---|---|---|
| 0 | 0 | medium (default) |
| 0 | 1 | low |
| 1 | 0 | high |
| 1 | 1 | medium SR <SR< high SR |

Delaying a channel's turn-On instant with respect to the other is accomplished by setting bits D2:D0 of the PWMR_s register to the appropriate values. Switch On is delayed by the number of (internal/external) clock periods shown in Table 8. See section Programmable PWM module.

## 6.3.8 Address $A_0$100— overcurrent protection configuration register (OCR_s)

The contents of the OCR_s registers determines operation of overcurrent, current sensing, and PWM related functions. For each load type (bulb or DC motor), a different kind of overcurrent profile exists (see Overcurrent protection profile for bulb applications). For lighting mode, the overcurrent profile is defined by three different thresholds each of which is active over a dedicated time slot. These thresholds are called the higher (=$I_{_OCH}$), the middle (=$I_{_OCM}$) and the lower (=$I_{_OCL}$) threshold. The DC motor profile only has two thresholds ($I_{_OCH}$ and $I_{_OCL}$).

Each threshold can be set to two different values, except $I_{_OCL}$ that can be set to three different values ($I_{_OCL1}$, $I_{_OCL2}$, $I_{_OCL3}$). Setting the low-current sense ratio (CSR1) reduces the values of all the overcurrent thresholds by a factor of three. The terminology is defined as follows: $I_{_OCxy_z}$ stands for overcurrent threshold x (x=$I_{_OCH}$, $I_{_OCM}$ or $I_{_OCL}$) that can be set to two or three different values, selected by

y (y=1, 2, (or 3)). The previously selected current sense ratio (z=0 for CSR0 and z=1 for CSR1) further determines the shape of the applicable overcurrent protection profile (see I_OCH1_0).

Setting bit D8 (HOCR_s) to 0 activates overcurrent level $I_{OCL1}$, the highest of the 3 levels, regardless the value of the D0 bit. Setting HOCR to 1 activates the medium level $I_{OCL2}$ when D0 = 0, and the lowest level $I_{OCL3}$ when D0 = 1 (Table 21). When overcurrent windows are active, current sensing is not available.

Bit D7 (PR_s) controls which of two divider values are used to create the PWM frequency from the external clock. Setting bit D7 to 1 causes the external clock to be divided by 512. When PR_s = 0, the divider is 256.

Setting bit D6 (Clock_int_s) activates the internal clock of the selected channel. The default value [0] configures the PWM module to use an external clock signal.

Setting bit D5 (CSNS_ratio_s) to 1 activates the “low- current” current sense ratio CSR1, optimal for measuring currents in the lowest range. The default value [0] activates the “high-current” sensing ratio CSR0 (Table 17).

**Table 17. Current sense ratio selection**

| CSNS_ratio_s (D5) | Current sense ratio |
|---|---|
| 0 | CRS0 (default) |
| 1 | CRS1 |

The width of the overcurrent protection window(s) is controlled by bits D4 and D3 ($t_{OCH_s}$ and $t_{OCM_s}$), and also depends on the load type configuration as shown in Table 18. (CONF[x]=0: bulb, CONF[x]=1: DC motor).

The lighting profile has two adjacent windows the width of which is compatible with typical bulb inrush current profiles. The width of the first of these windows is either $t_{OCH1}$ or $t_{OCH2}$. The width of the second window is either $t_{OCM1_L}$ or $t_{OCM2_L}$ (see Table 18).

The DC motor profile has one overcurrent window defined by two different thresholds ($I_{OCH}$ and $I_{OCL}$), as illustrated by Figure 6. In this case, the maximum overcurrent duration is selected among four values: $t_{OCM1_M}$, $t_{OCM2_M}$, $t_{OCH1}$ and $t_{OCH2}$.

**Table 18. Dynamic overcurrent threshold activation times for bulb and DC motor profiles**

| CONF[x] | $t_{OCH_s}$ (D4) | $t_{OCM_s}$ (D3) | Selected threshold activation times |
|---|---|---|---|
| 0 | 0 | 0 | $t_{OCH1}$ and $t_{OCM1_L}$ |
| 0 | 0 | 1 | $t_{OCH1}$ and $t_{OCM2_L}$ |
| 0 | 1 | 0 | $t_{OCH2}$ and $t_{OCM1_L}$ |
| 0 | 1 | 1 | $t_{OCH2}$ and $t_{OCM2_L}$ |
| 1 | 0 | 0 | $t_{OCM1_M}$ |
| 1 | 0 | 1 | $t_{OCM2_M}$ |
| 1 | 1 | 0 | $t_{OCH1}$ |
| 1 | 1 | 1 | $t_{OCH2}$ |

Bit D2 (OCH_s) selects the value of the higher (upper) overcurrent threshold among two values. The default value [0] corresponds to the highest value, and [1] to the lowest value (Table 19).

**Table 19. OCH upper current threshold selection**

| OCH_s (D2) | $I_{OCH}$ Current Threshold |
|---|---|
| 0 | $I_{OCH1_s}$ (default) |
| 1 | $I_{OCH2_s}$ |

Bit D1 (OCM_s) sets the value of the middle overcurrent threshold. The default value [0] corresponds to the highest value, and [1] to the lowest value (Table 20). In DC motor mode, there is no middle overcurrent threshold and the value of this bit has no influence.

**Table 20. OCM current threshold selection**

| OCM_s (D1) | OCM current threshold |
|---|---|
| 0 | $I_{OCM1_s}$ (default) |
| 1 | $I_{OCM2_s}$ |

Bit D0 (OCL_s) and D8 (HOCR) set the value of the lowest overcurrent threshold, as shown in Table 21.

**Table 21. OCL current threshold selection**

| HOCR (D8) | OCL_s (bit D0) | Selected OCL current level |
|---|---|---|
| 0 | 0 | $I_{_OCL1_x}$(default) |
| 0 | 1 | $I_{_OCL1_x}$ |
| 1 | 0 | $I_{_OCL2_x}$ |
| 1 | 1 | $I_{_OCL3_x}$ |

## 6.3.9 Address $A_0$101— Auto-retry register (RETRYR_s)

The RETRYR_s register contents are used to set the different auto-retry options (Auto-retry), the offset compensation feature of the current sense function, and the overcurrent profile.

Setting bit D8 to 1(OFP = 1) causes the random offset current to be added to the sensed current (pin CSNS). Setting bit D8 to 0 results in the offset current being subtracted from the sensed current. Setting D3 and D2 (Table 22) to the appropriate values allows selection of the value of the auto-retry period among four predefined values.

**Table 22. Auto-retry period**

| Auto_period1_s (D3) | Auto_period0_s (D2) | Retry period |
|---|---|---|
| 0 | 0 | $t_{AUTO_00}$ (default) |
| 0 | 1 | $t_{AUTO_01}$ |
| 1 | 0 | $t_{AUTO_10}$ |
| 1 | 1 | $t_{AUTO_11}$ |

Setting bit D1 to 1 (RETRY_unlimited_s = 1) results in an unlimited number of auto retries, provided the auto-retry function wasn't disabled.

Setting bit D1 to 0 (RETRY_unlimited_s = 0) limits the amount of auto retries to 16 (see Amount of auto-retries). The value of the counter neither resets after delatching, nor when the fault disappears.

Setting bit D0 (retry_s) enables or disable auto-retry, accordingly to setting of the CONF pin.

For CONF[x] = 0 (Lighting profile configured), setting retry_s = 1 disables auto-retry. The default value [0] enables it.

For CONF[x] = 1 (DC motor), setting retry_s = 1 enables auto-retry. The default value [0] disables it.

Setting bit D4 to 0 (CONF_SPI_s = 0) will configure the overcurrent profile as the CONF pin.

Setting bit D4 to 1 (CONF_SPI_s = 1) will configure the overcurrent profile as the opposite of the CONF pin.

## 6.3.10 Address 0110—global configuration register (GCR)

The GCR register is used to activate various functions and diagnostic functions.

Setting bits D8 = 1 and D7 = 1 of the GCR register (PWM_en_1 and PWM_en_0) activates the internal PWM function of both channels simultaneously according to the values of duty cycle and turn-on delays in the PWMR_s and CONFR_s registers (Table 7). However, this option should never be used to drive channels in parallel. To increase the load current capability, the instructions in the section Parallel operation should be followed.

Setting bit D6 sets Parallel mode (improved switching synchronization between both channels). Only configuration and diagnostic information of bank 0 ($A_0$ = 0) is available in this setting (see Parallel operation).

Setting Bit D5 (T_H_en = 1) activates Track & Hold current sensing mode. When T&H is activated, the value of the channel's load current is kept available after turn-off.

Setting bit D4 (WD_dis = 1) disables the SPI watchdog function. A logic [0] enables the SPI watchdog.

Setting bit D3 ($V_{DD_FAIL_EN}$ = 1) enables or disable the $V_{DD}$ failure detection. When enabled, the device enters Fail-safe mode after $V_{DD}$ < $V_{DD(FAIL)}$.

Bits D6 (parallel bit), D2 and D1 set the different (current) sensing options. The CSNS pin outputs a scaled value of the selected channel's load current, the sum of both currents or the die temperature, according to the values in Table 23. When the highest overcurrent range is selected (bit D8 of the OCR register, HOCR = 0), the device's CSNS pin only outputs scaled values of a single channel's load current.

**Table 23. Current sense pin functionality selection**

| D8 | D6 | D2 | D1 | Activated function at CSNS pin |
|---|---|---|---|---|
| x | x | 0 | 0 | disabled |
| 0 | x | 0 | 1 | current sensing on channel 0 |
| 0 | x | 1 | 0 | current sensing on channel 1 |
| 0 | x | 1 | 1 | temperature sensing |
| 1 | 0 | 0 | 1 | current sensing on channel 0 |
| 1 | x | 1 | 0 | current sensing on channel 1 |
| 1 | x | 1 | 1 | temperature |
| 1 | 1 | 0 | 1 | current sensing summed currents of channels 0 and 1 |

Setting bit D0 (OV_dis = 1 of the GCR reg.) disables overvoltage protection. Setting this bit to [0] (default), enables it.

## 6.3.11 Address $A_0111$—Calibration register (CALR_s)

The internal clock frequency of both channels can be calibrated independently. Setting the appropriate calibration word in the CALR_s register (Table 12) puts the device in calibration mode. The default switching frequency is 400 Hz, but can be changed by applying a specific calibration procedure. See Internal clock and internal PWM (Clock_int_s bit = 1).

## 6.3.12 SO register addressing

The device has two register banks, each of which has five channel-specific SO registers containing the channel's configuration and diagnostics status (Table 13). These registers are FAULTR_s, PWMR_s, CONFR_s, OCR_s, and RETRYR_s.

Global fault and diagnostic information are contained in the following common SO-registers: STATR, GCR, and DIAGR. All the SO registers can be addressed by setting the appropriate bits in the SI-STATR_s register (bits D13, D2, D1, D0). The value of the bit D13 determines which register bank is addressed (bank 0 or 1). Data is made available the next cycle after register addressing. The output status register correctly reflects the contents of the addressed SO register as long as CSB is low, except when the data from the previous SPI cycle was invalid. In this case, the device outputs the contents of the last successfully addressed SO register.

## 6.3.13 Serial output register assignment

The output register shifted out through the SO pin is previously addressed by bits D13, D2, D1, and D0 of the STATR_s SI register. Table 13 gives the functional assignment (OD15:OD0) of each of the thirteen SO register bits, preceded by the address of the SI STATR_s required to address it.

- Bit OD15 (MSB) reports the state of the watchdog bit from the previously clocked-in SPI message.
- Bit OD14 (PF, active 1) reports an eventual parity error on the previously transferred SI register contents.
- Bits OD13:OD10 echo the state of bits D13, D2, D1, and D0 (SOA3:SOA0) of the previously received SI word.
- Bit OD9: Normal mode (NM) reports the device state. In Normal Mode, NM = 1.
- Bits OD8:OD0 are the contents of the selected SO register (addressed by bit D13 and bits D2:D0 of the previous SI STATR register).

## 6.3.14 Previous address $SOA_3$:$SOA_0$ = 0000 (STATR)

When bits SOA3…SOA0 of the previously received SI STATR_s register = 0000, the SO STATR register is addressed. Bits OD8:OD0 contain the relevant channel information: Faults, channel state, and supply voltage errors.

- Bits OD8:OD6 report failures common to both channels
- Bit OD8 = OV = 1: overvoltage fault
- Bit OD7 = UV = 1: undervoltage fault
- Bit OD6 = POR = 1: power-on reset (POR) has occurred

Power-ON-Reset occurs when $V_{PWR}$<$V_{SUPPLY(POR)}$. The OV, UV, and POR bits can be reset by a reading the STATR register. Bits OD5:OD4 ($R_{FULL}$) of the STATR register are set to logic [1] when the auto-retry counter of the corresponding channel is full. These bits are automatically cleared by resetting the corresponding auto-retry counter (see Reset of the auto-retry counter). Bits OD3 (FAULT1) and OD2 (FAULT0) are set to logic [1] when channel-specific (non-generic) faults are detected:

FAULTs = OC_s + SC_s + OT_s + OS_s + OLOFF_s + OLON_s.

The FAULTs bit can be reset by reading out the common STATR register or the individual FAULTR_s register (provided the fault has disappeared).

Bits OD1:OD0 (OUT1 and OUT0) report the channel's switching state (On/Off) in real time.

## 6.3.15 Previous address $SOA_3$:$SOA_0$ = $A_0$001 (FAULTR_s)

Bit OD8 of both Fault registers (FAULTR_s) is set simultaneously when the overtemperature prewarning (OTW) condition occurs, but the channels are not switched off (temperature of the common GND pins (8 and 25)> $T_{OTWAR}$). Reading either FAULT register clears both OTW bits.

Bits OD5:OD0 of the Fault register (FAULTR_s) report the faults that occurred on the channel previously selected by bit SOA3 = $A_0$ (Table 14).

- bit OD0 = OC_s: overcurrent fault on channel s,
- bit OD1 = SC_s: severe short-circuit on channel s,
- bit OD3 = OS_s: output shorted to $V_{PWR}$ on channel s,
- bit OD4 = OLOFF_s: open load in OFF state on channel s,
- bit OD5 = OLON_s: open load in ON state on channel s. (The threshold value above which this fault is triggered depends on the selected current sense ratio; for CSR0 at 150 mA typ. and for CSR1 at 7.0 mA typ.).

The Fault Status pin (FSB) is set to 0 (active Low) upon occurrence of any of the above mentioned faults. Latched faults can only be delatched by the procedure described in Fault delatching. The FAULTR_s register is reset when it is read out, provided that the failure cause has disappeared and latched faults have been delatched.

## 6.3.16 Previous address $SOA_3$:$SOA_0$ = $A_0$010 (PWMR_s)

The device outputs the contents of the addressed PWMR_s register ($A_0$ = 0 for bank 0 and $A_0$ = 1 for bank 1).

## 6.3.17 Previous address $SOA_3$:$SOA_0$ = $A_0$011 (CONFR_s)

The device outputs the contents of the addressed CONFR_s register ($A_0$ = 0 for bank 0 and $A_0$ = 1 for bank 1).

## 6.3.18 Previous address $SOA_3$:$SOA_0$ = $A_0$100 (OCR_s)

The device outputs the contents of the addressed OCR_s register ($A_0$ = 0 for bank 0 and $A_0$ = 1 for bank 1).

## 6.3.19 Previous address $SOA_3$:$SOA_0$ = $A_0$101 (RETRYR_s)

The device outputs the contents of the addressed RETRYR_s register ($A_0$ = 0 for bank 0 and $A_0$ = 1 for bank 1). Bit OD8 contains the value of the OFP bit (offset positive), used for current sense offset compensation. Bits OD7:OD4 contain the real time value of the auto-retry counter. When these bits contain [0000], either auto-retry has not been enabled or Auto-retry did not occur.

## 6.3.20 Previous address $SOA_3$:$SOA_0$ = 0110 (GCR)

The device outputs the contents of the general configuration register (GCR) common to both channels.

## 6.3.21 Previous address $SOA_3$:$SOA_0$ = 0111 (DIAGR_s)

Bit OD8 ( Ch. 1 = CONF1) and bit OD7 ( Ch. 0 = CONF0) of the DIAGR_s register contain the values of the channels' configuration bits (0 = bulb, 1 = DC motor)

Bits OD6:OD5 contain the product identification (ID) number, equal to 00 for the present dual 22 mΩ product.

Bits OD4:OD3 report the logic state of the direct inputs IN[1:0] in real time (1 = On, 0 = OFF), OD4 = Ch. 1, OD3 = Ch. 0.

Bit OD2 reports a logic [1] in case an external clock error occurred (if an external clock was selected by Clock_int = 0)

Bit OD1:OD0 report logic [1] in case a calibration failure occurred during calibration of a channel's internal clock period.

# 7 Typical applications

Figure 24 shows the electrical circuit of a typical truck application. As an example, an external circuit is added that takes over load control in case Fail-safe mode is activated (FSOB goes low). This circuit allows keeping full control of both channels in case of SPI failure.

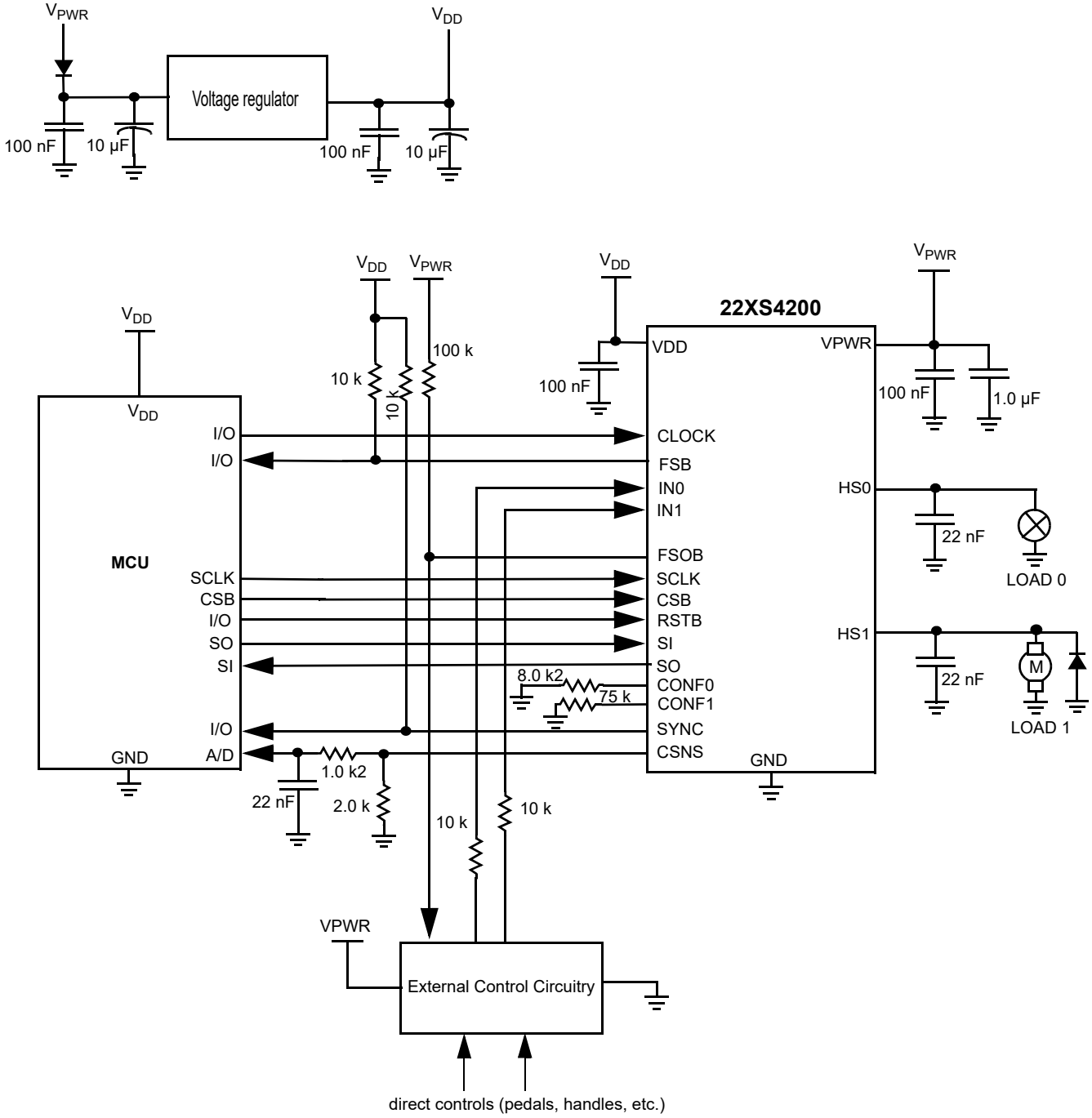



**Figure 24. Typical application with two different load types**

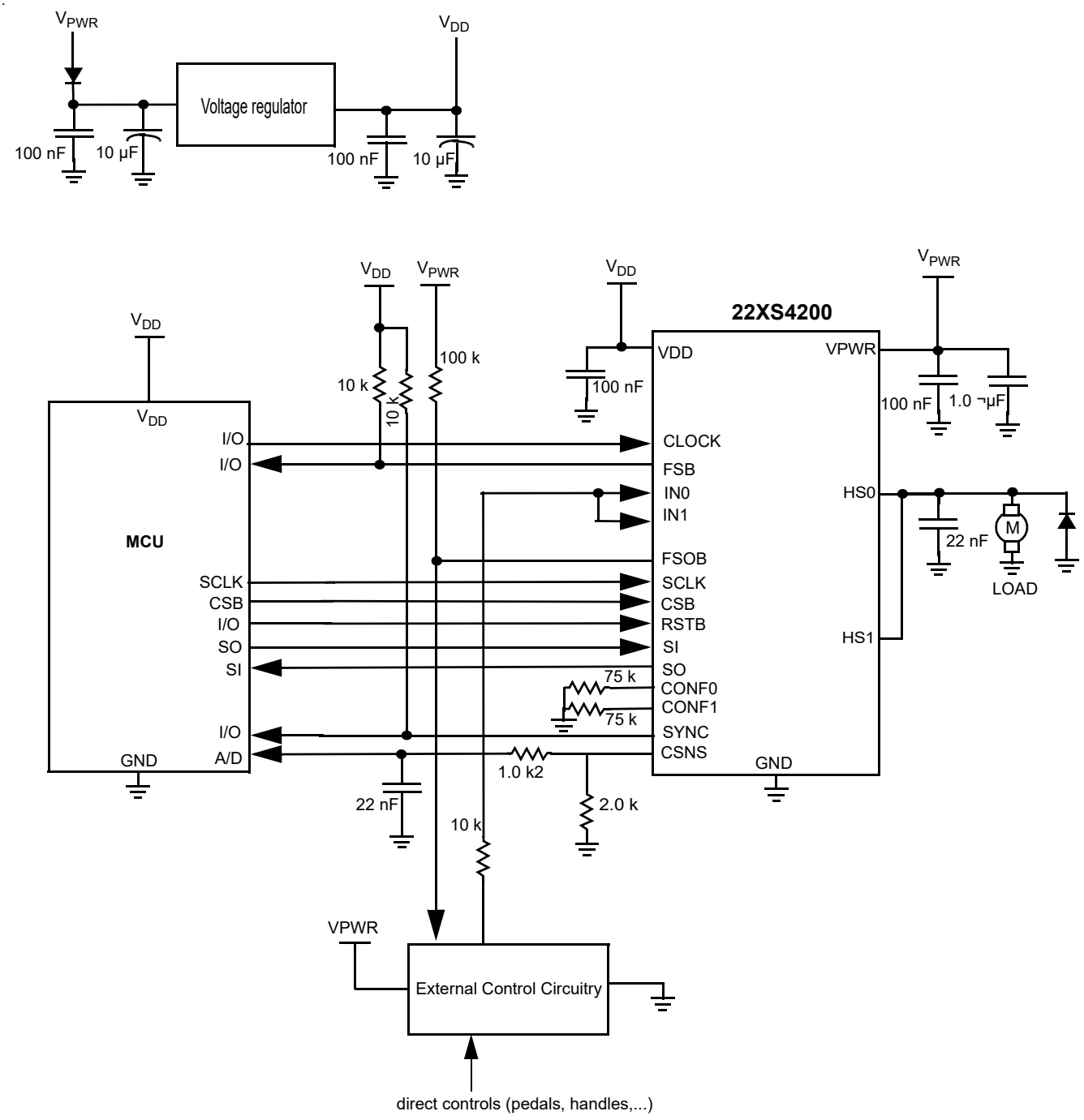


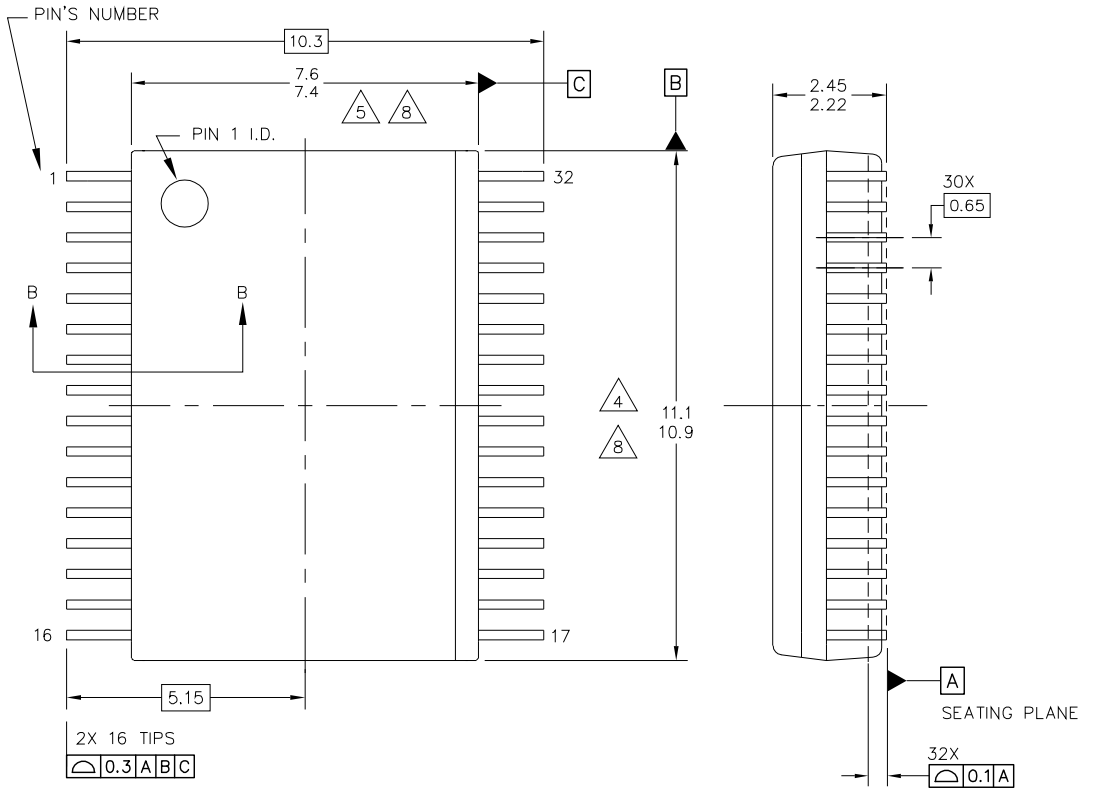

**Figure 25. Two channels in parallel / recommended external current sense circuit**

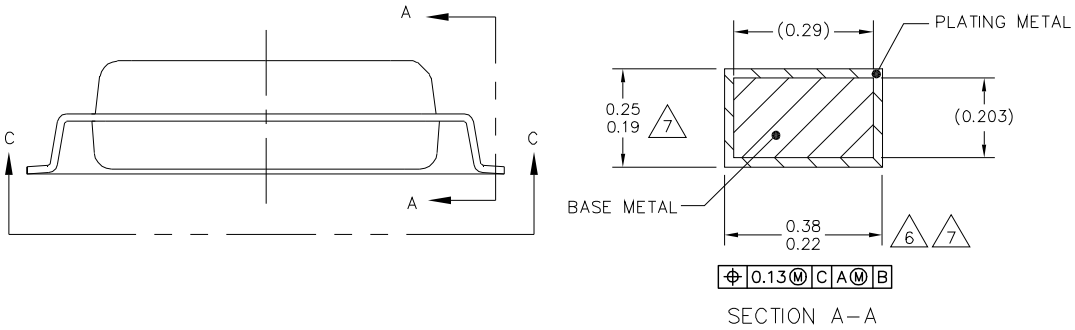
# 8 Packaging

## 8.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

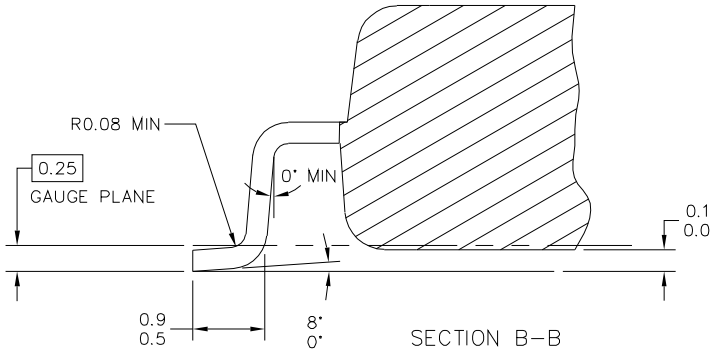
| Package | Suffix | Package outline drawing number |
|---|---|---|
| 32 Pin SOIC-EP | BEK | 98ASA00368D |
| | CEK | 98ASA00894D |



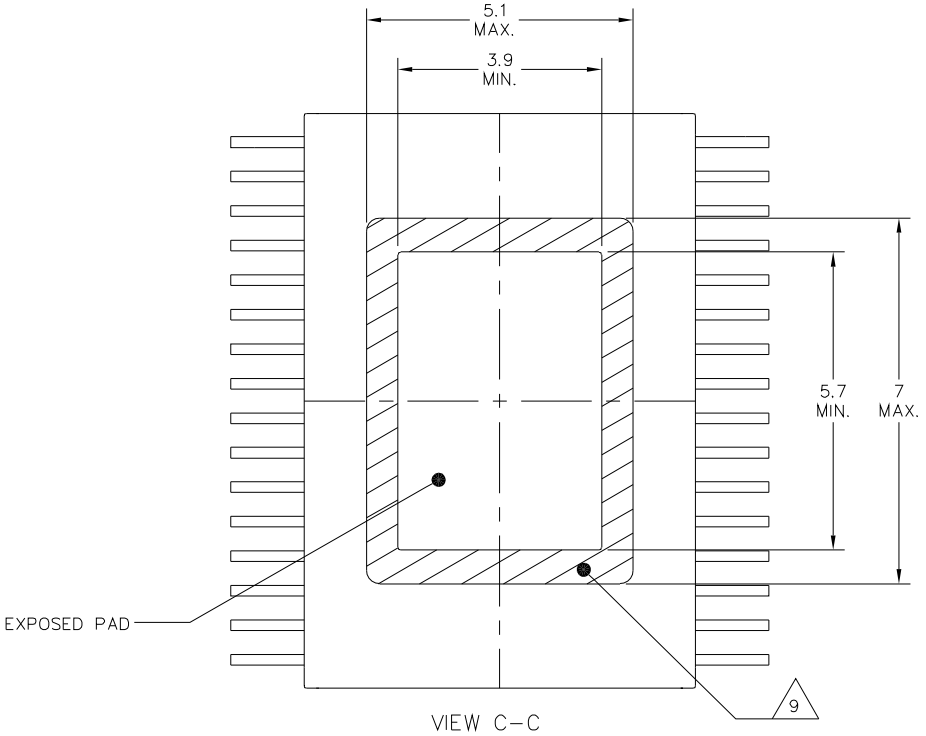




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SECTION B–B




VIEW C–C

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| | STANDARD: NON–JEDEC | |
| | SOT1746–2 | 07 JAN 2016 |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
8. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
9. HATCHED AREA TO BE KEEP–OUT ZONE FOR PCB ROUTING.

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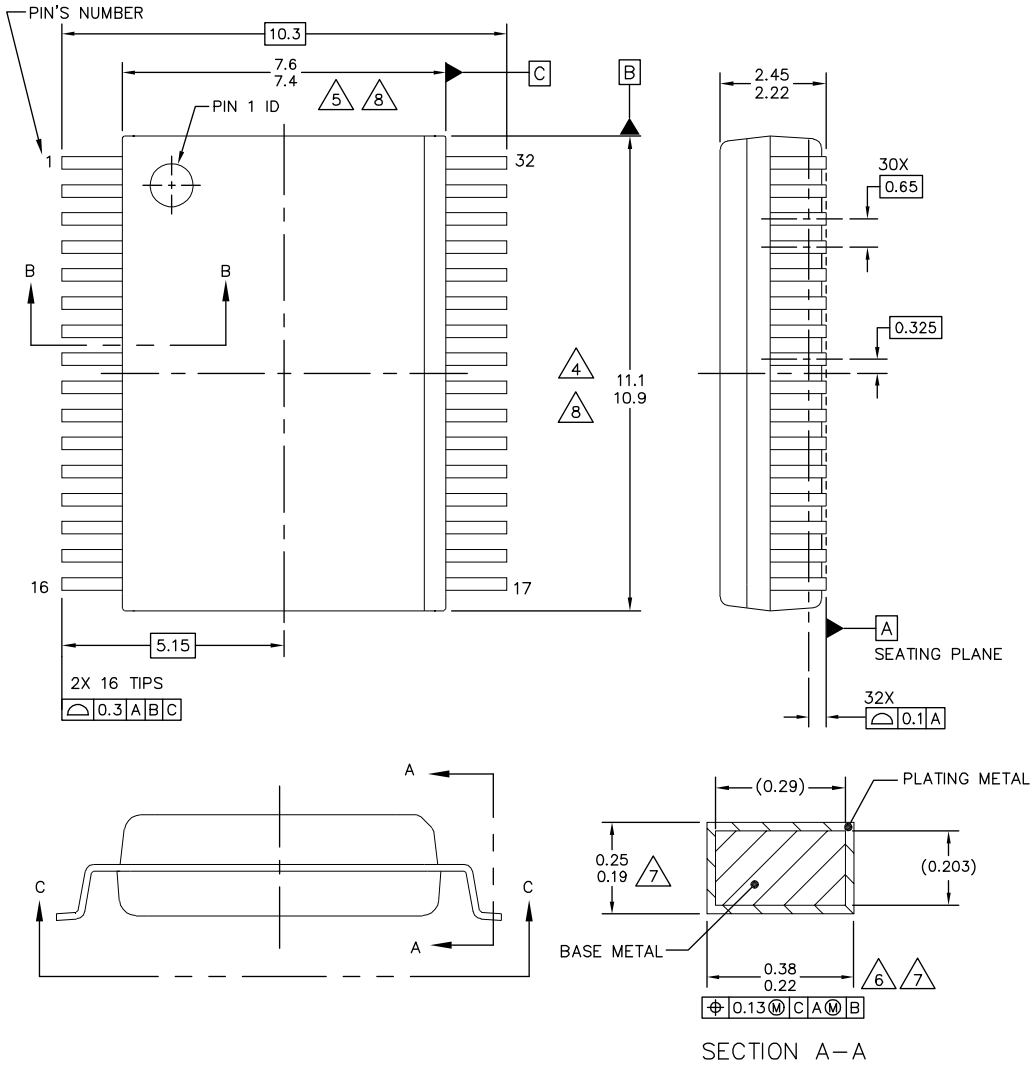
| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
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| TITLE: | DOCUMENT NO: 98ASA00368D | REV: A |
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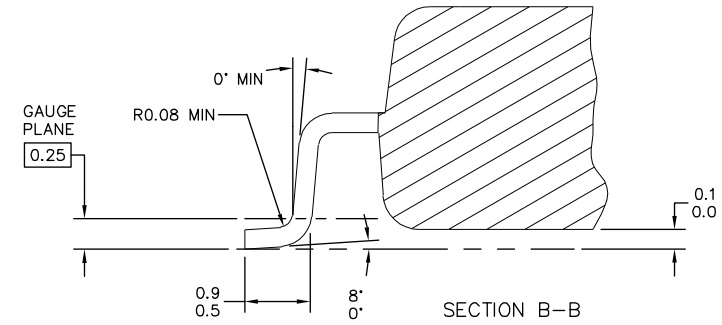



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|---|---|---|
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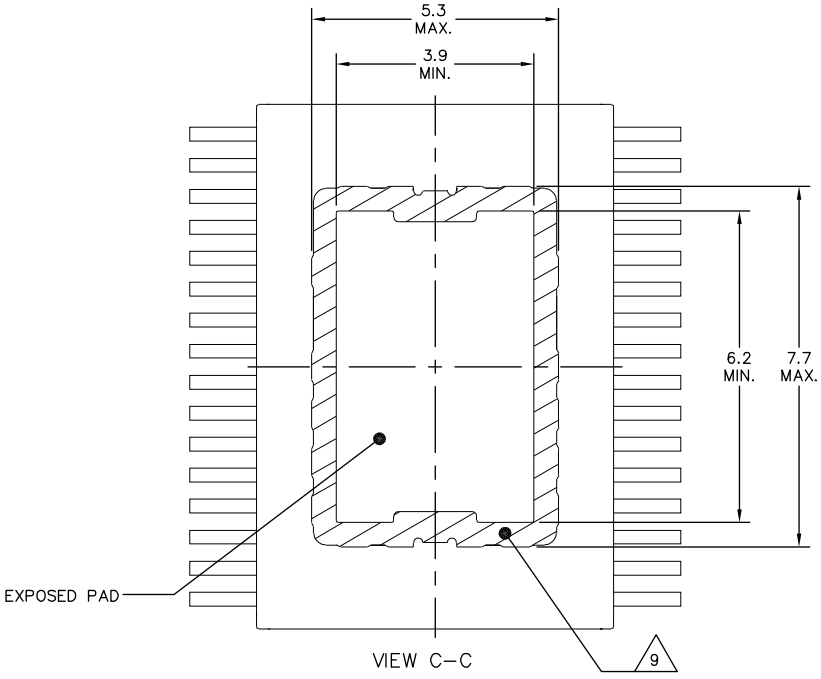
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VIEW C–C

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9. HATCHED AREA TO BE KEEP–OUT ZONE FOR PCB ROUTING.

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| | SOT1746–4 | SHEET: 3 |

# 9 Revision history

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 3/2014 | • Initial release |
| 2.0 | 9/2014 | • Updated turn-on and turn-off delay time<br>• Updated overcurrent detection thresholds<br>• Updated output current sensing error |
| 3.0 | 1/2015 | • Thermal parameter update per PB#16607 |
| | 8/2016 | • Updated to NXP document form and style |
| 4.0 | 5/2018 | • Updated as per CIN 201805020I<br>• Changed steady-state current value from 3.0 to 4.2 A listed under features on page 1<br>• Updated $I_{HS[0:1]}$ value in Table 3 (changed 3.0 to 4.2)<br>• Added clarification for diagnostic range to Table 5<br>• Corrected typo in Reverse voltage protection on VPWR (changed -28 V to -32 V)<br>• Updated load dump duration (changed 500 ms to 350 ms) and changed $V_{PWR}$ from 14 V to 28 V in Table 3<br>• Updated Track & Hold current sensing mode<br>• Changed “Bits OD6:OD5 contain the product identification (ID) number, equal to 01 for the present dual 22 mΩ product” to “Bits OD6:OD5 contain the product identification (ID) number, equal to 00 for the present dual 22 mΩ product” in Previous address SOA3:SOA0 = 0111 (DIAGR_s) |
| 5.0 | 6/2018 | • Added MC22XS4200CEK part to Table 1 and associated 98ASA00894D package information |

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6/2018